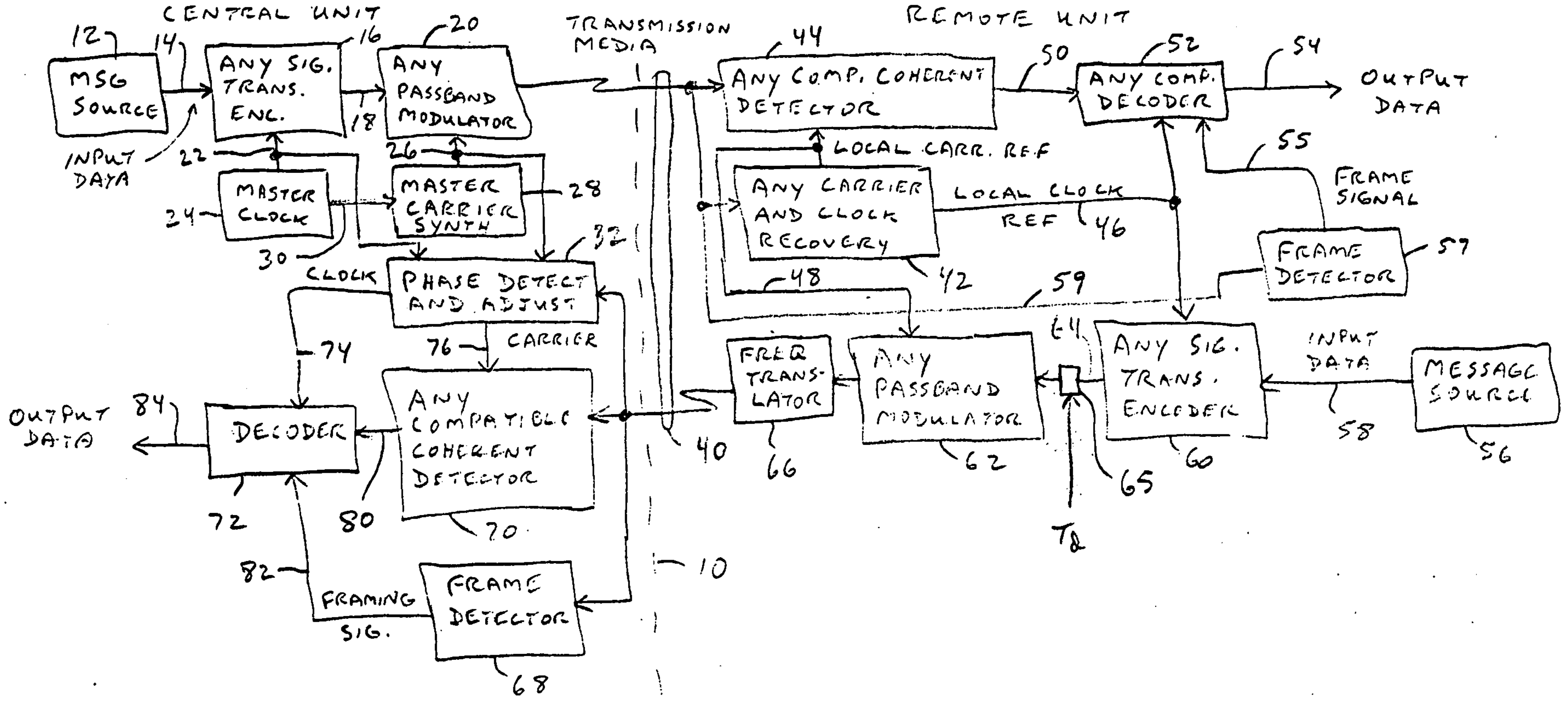
Sent to Di
July 97



CENTRAL UNIT
REMOTE UNIT
12
MSG SOURCE
14
INPUT DATA
16
ANY SIG. TRANS. ENC.
18
20
ANY PASSBAND MODULATOR
22
24
MASTER CLOCK
26
MASTER CARRIER SYNTH
28
30
32
CLOCK
PHASE DETECT AND ADJUST
74
76
CARRIER
ANY COMPATIBLE COHERENT DETECTOR
70
OUTPUT DATA
84
DECODER
72
80
82
FRAMING SIG.
FRAME DETECTOR
68
TRANSMISSION MEDIA
10
40
44
ANY COMP. COHERENT DETECTOR
50
52
ANY COMP. DECODER
54
OUTPUT DATA
LOCAL CARR. REF
ANY CARRIER AND CLOCK RECOVERY
42
LOCAL CLOCK REF
46
55
FRAME SIGNAL
FRAME DETECTOR
57
48
59
FREQ TRANS-LATOR
66
ANY PASSBAND MODULATOR
62
64
65
T_d
ANY SIG. TRANS. ENCODER
60
INPUT DATA
58
MESSAGE SOURCE
56

FIG. 1

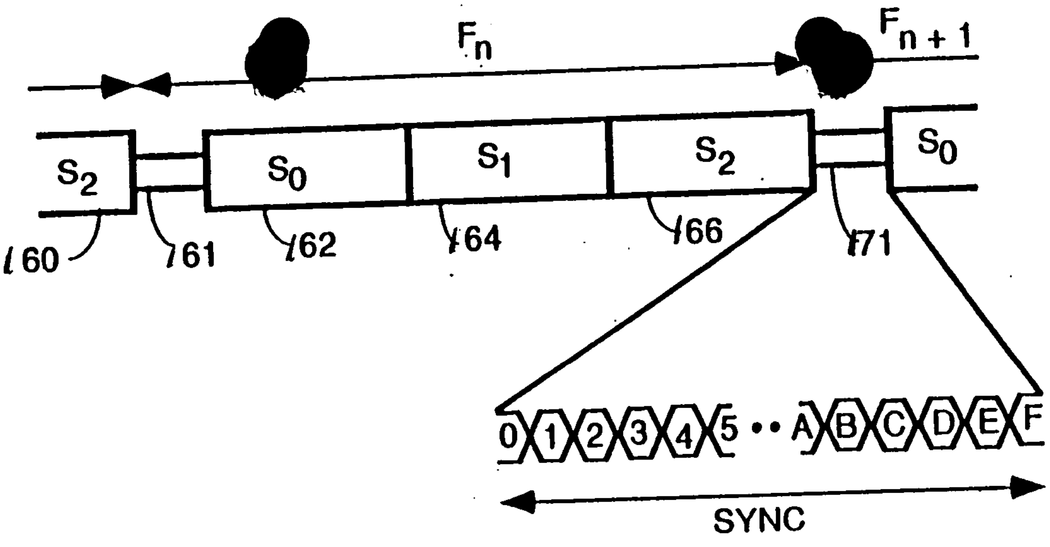

F_n
F_{n+1}
S_2
S_0
S_1
S_2
S_0
160
161
162
164
166
171
0 1 2 3 4 5 •• A B C D E F
SYNC

FIG. ~~4A~~ 2A

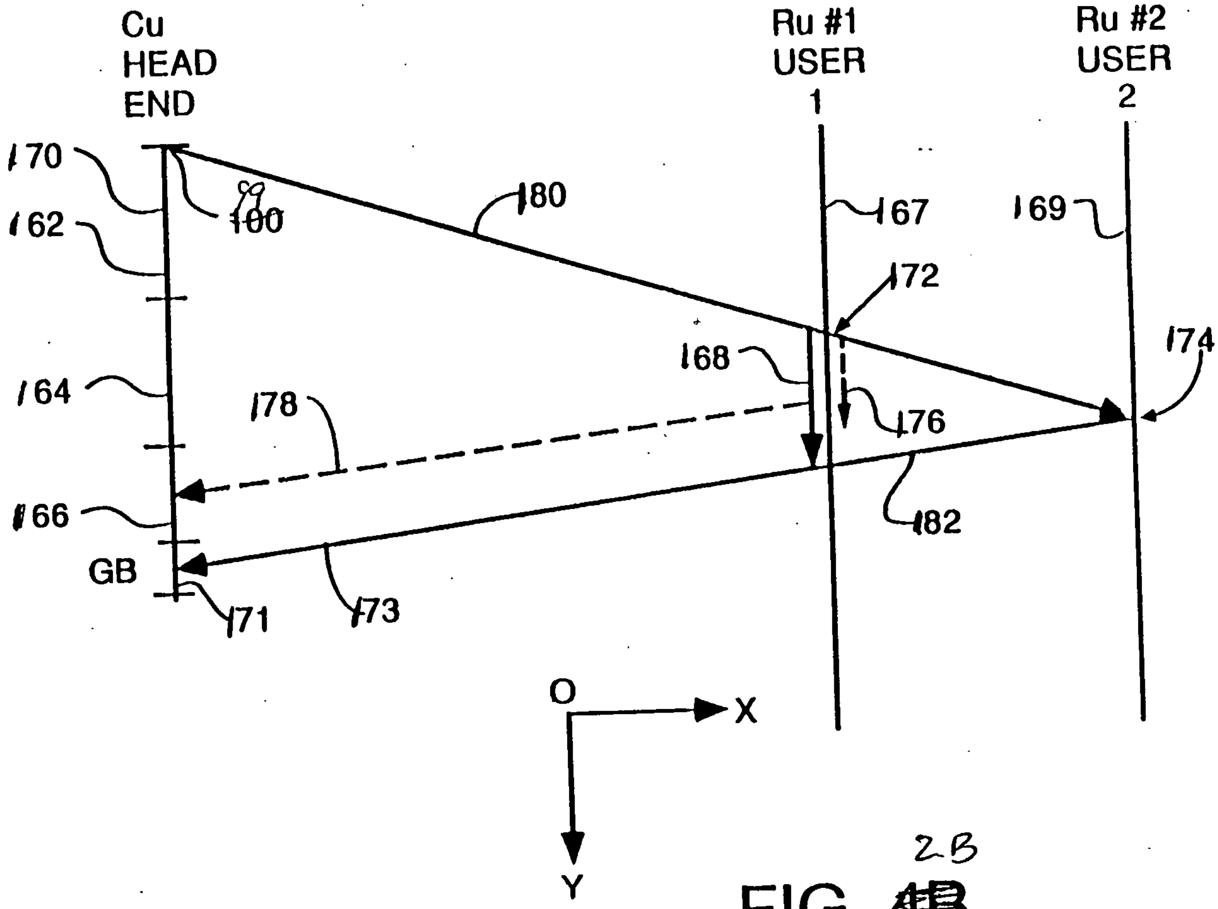

Cu
HEAD
END
Ru #1
USER
1
Ru #2
USER
2
170
162
164
166
GB
171
~~100~~ 99
180
167
169
172
174
168
176
178
182
173
O
X
Y

FIG. ~~4B~~ 2B

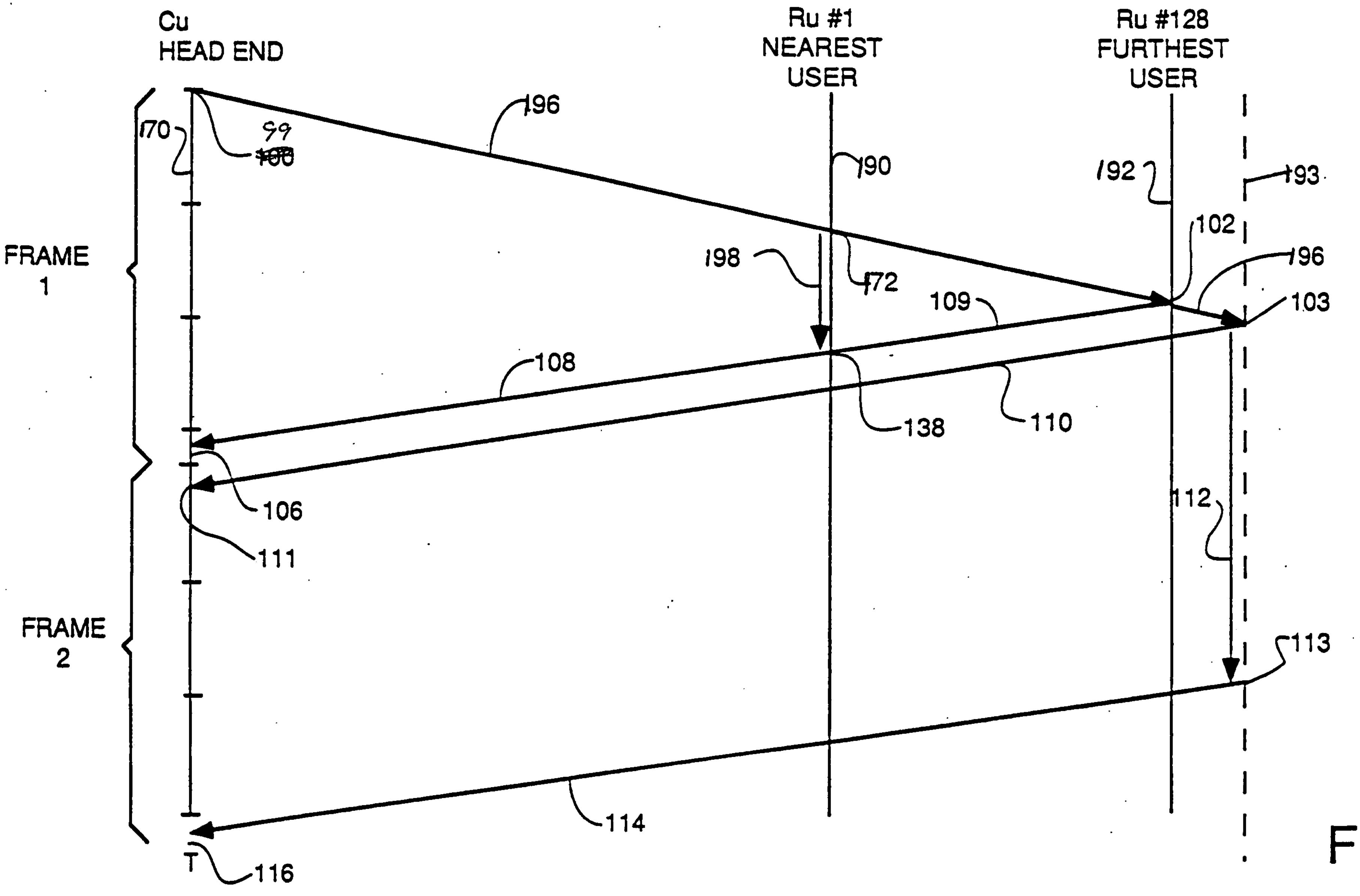

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
~~100~~
FRAME
FRAME

FIG. ~~5~~ 3

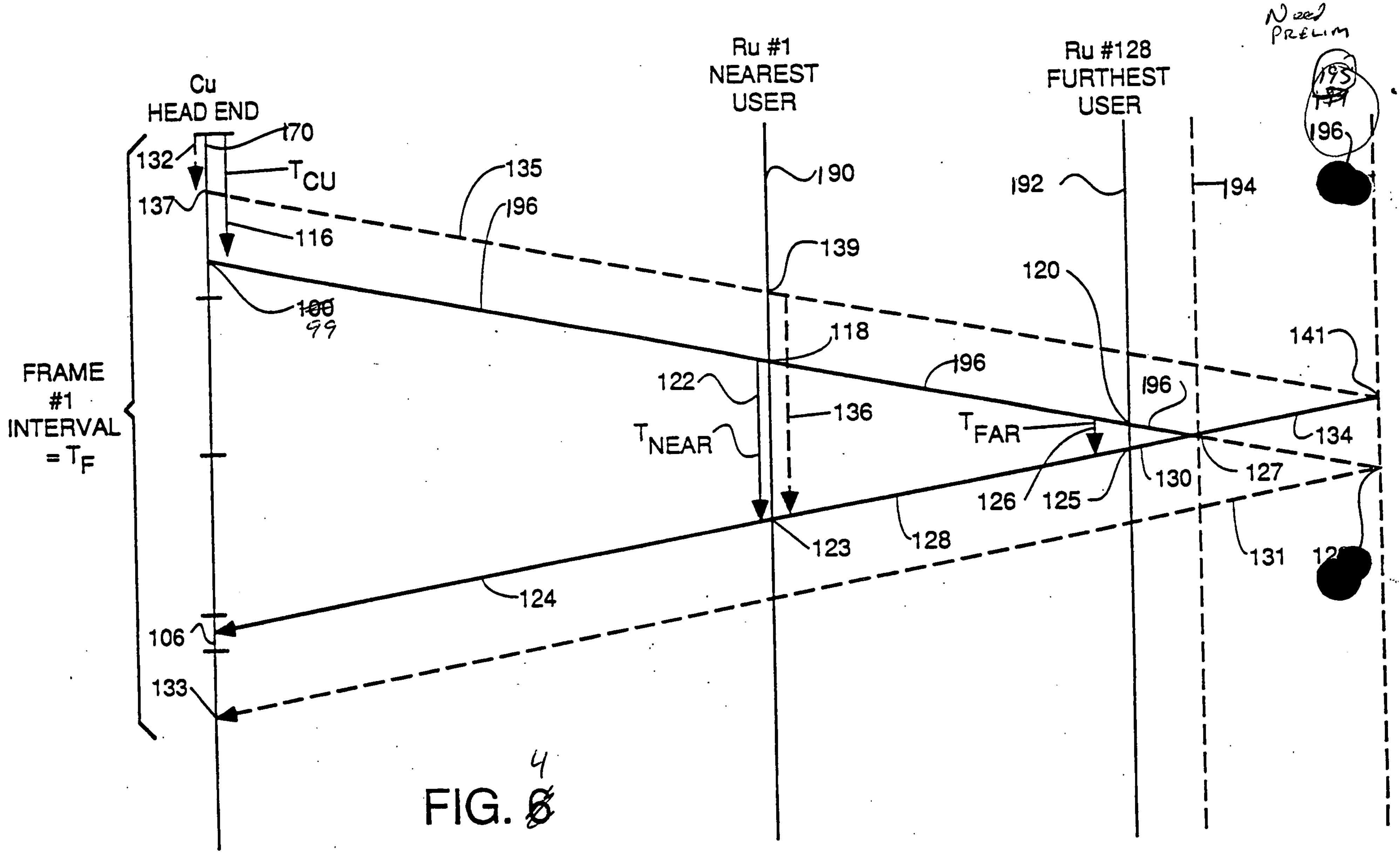
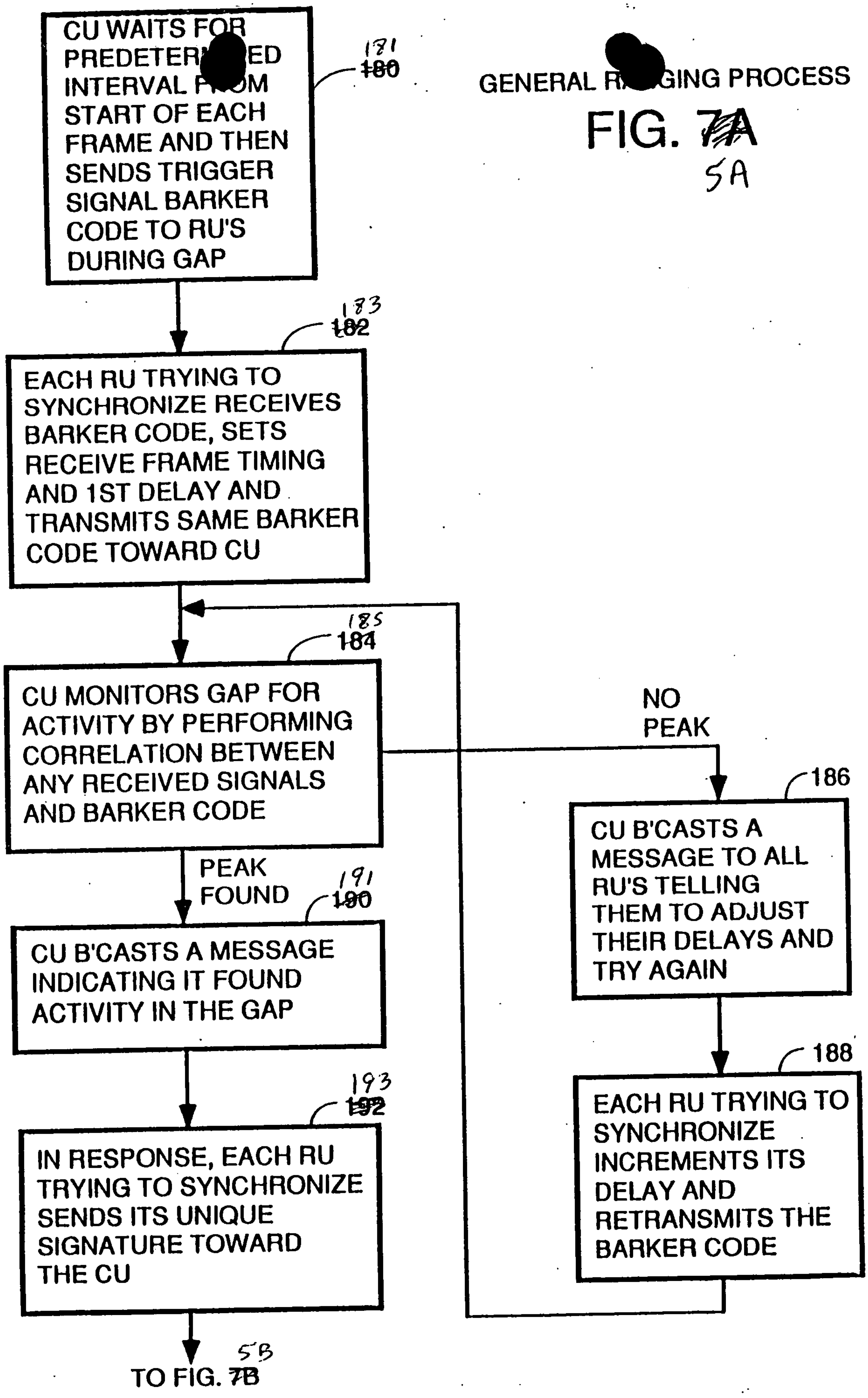
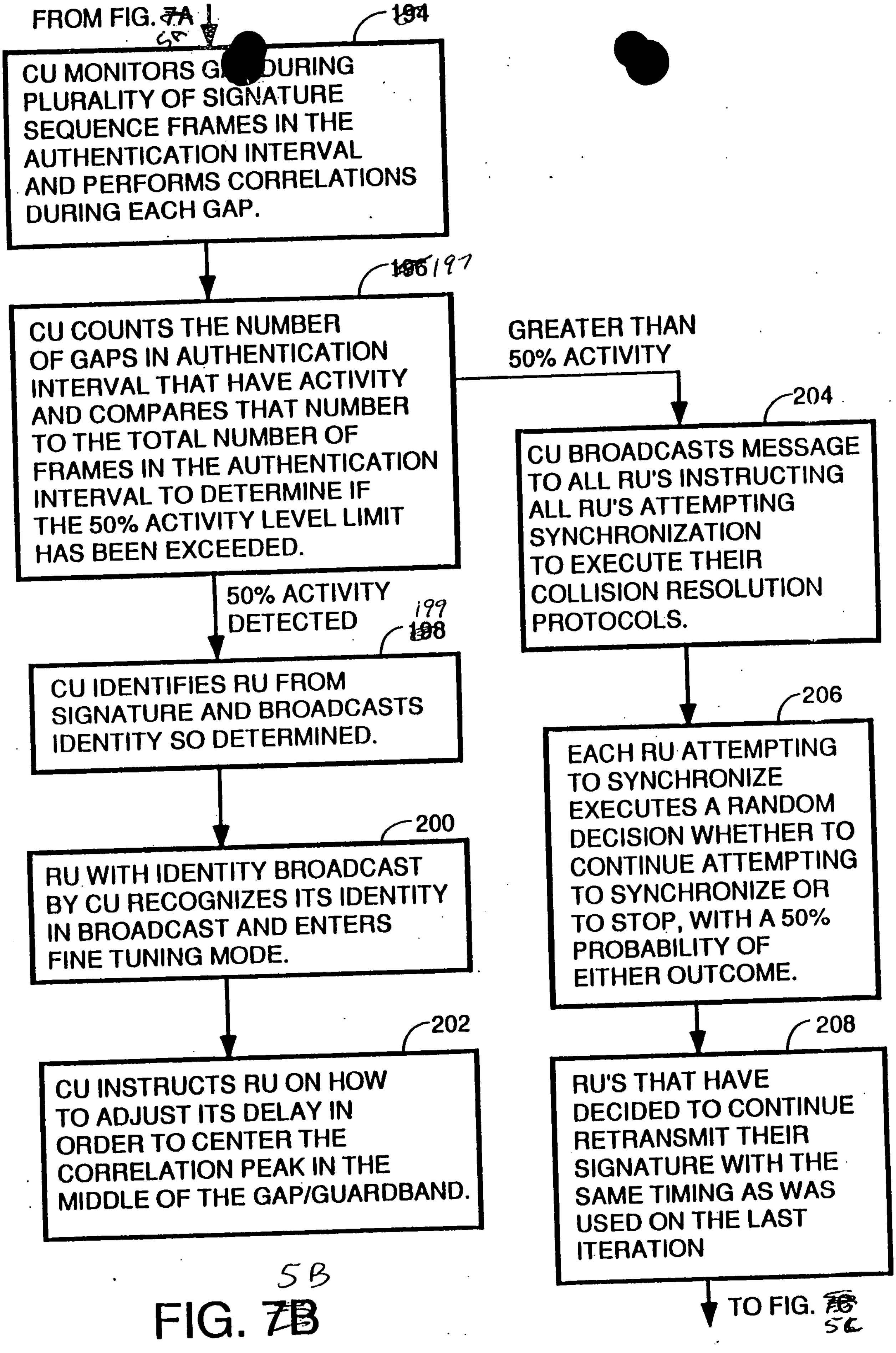

Need PRELIM
Cu
HEAD END
T_{CU}
~~100~~
FRAME
#1
INTERVAL
$= T_F$
Ru #1
NEAREST
USER
T_{NEAR}
Ru #128
FURTHEST
USER
T_{FAR}
~~199~~

FIG. ~~6~~ 4

GENERAL R[illegible]GING PROCESS

FIG. ~~7A~~ 5A


CU WAITS FOR PREDETER[illegible]ED INTERVAL F[illegible]OM START OF EACH FRAME AND THEN SENDS TRIGGER SIGNAL BARKER CODE TO RU'S DURING GAP
181
~~180~~
EACH RU TRYING TO SYNCHRONIZE RECEIVES BARKER CODE, SETS RECEIVE FRAME TIMING AND 1ST DELAY AND TRANSMITS SAME BARKER CODE TOWARD CU
183
~~182~~
CU MONITORS GAP FOR ACTIVITY BY PERFORMING CORRELATION BETWEEN ANY RECEIVED SIGNALS AND BARKER CODE
185
~~184~~
NO PEAK
186
CU B'CASTS A MESSAGE TO ALL RU'S TELLING THEM TO ADJUST THEIR DELAYS AND TRY AGAIN
188
EACH RU TRYING TO SYNCHRONIZE INCREMENTS ITS DELAY AND RETRANSMITS THE BARKER CODE
PEAK FOUND
191
~~190~~
CU B'CASTS A MESSAGE INDICATING IT FOUND ACTIVITY IN THE GAP
193
~~192~~
IN RESPONSE, EACH RU TRYING TO SYNCHRONIZE SENDS ITS UNIQUE SIGNATURE TOWARD THE CU
TO FIG. ~~7B~~ 5B


FROM FIG. ~~7A~~ 5A
~~194~~
CU MONITORS GAP DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
~~196~~ 197
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
GREATER THAN 50% ACTIVITY
204
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
50% ACTIVITY DETECTED
199
~~198~~
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
206
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
200
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
202
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.
208
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. ~~7C~~ 5C

5B

FIG. ~~7B~~

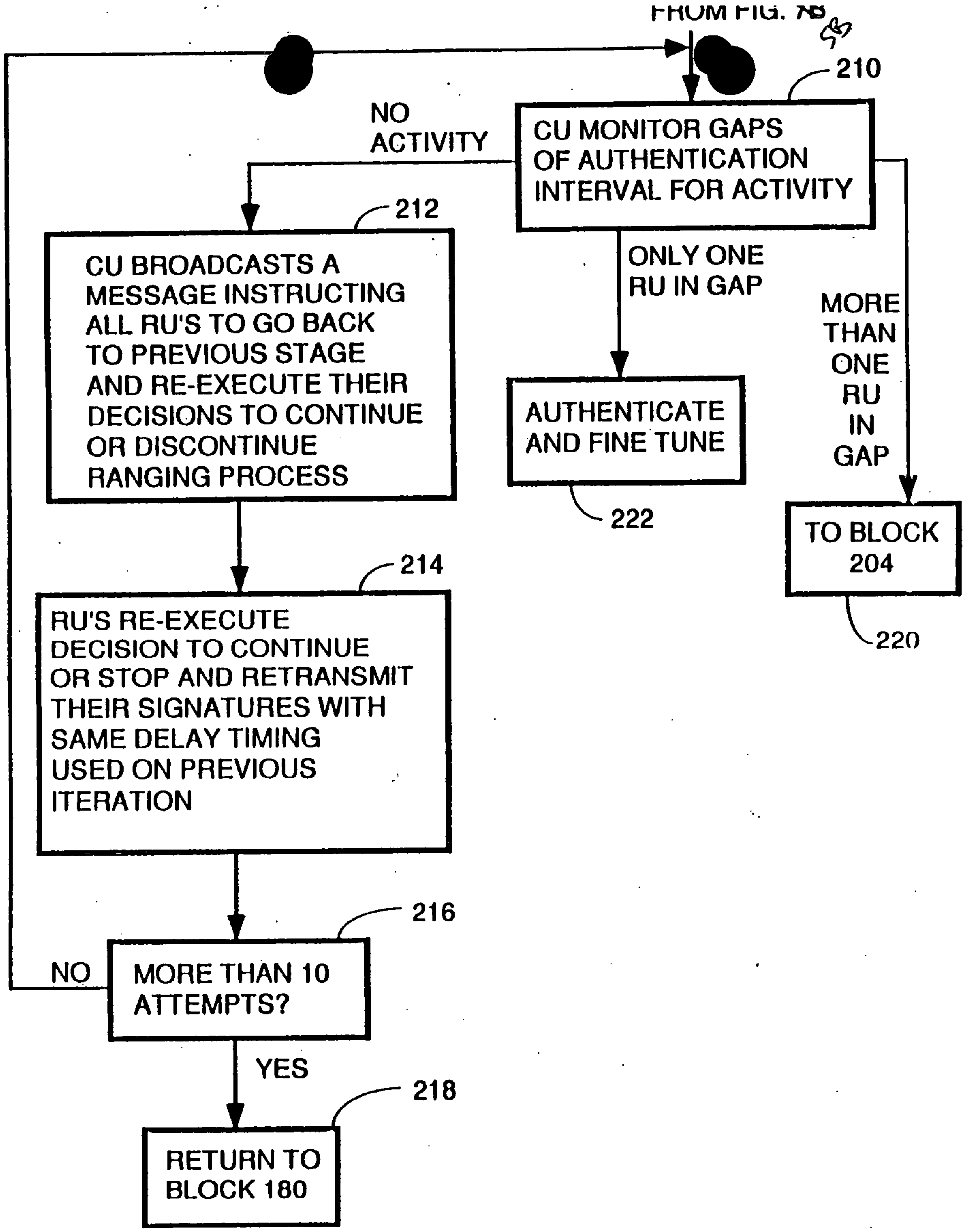

FROM FIG. ~~7B~~ 5B
210
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
NO ACTIVITY
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
ONLY ONE RU IN GAP
AUTHENTICATE AND FINE TUNE
222
MORE THAN ONE RU IN GAP
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. ~~7C~~ 5C

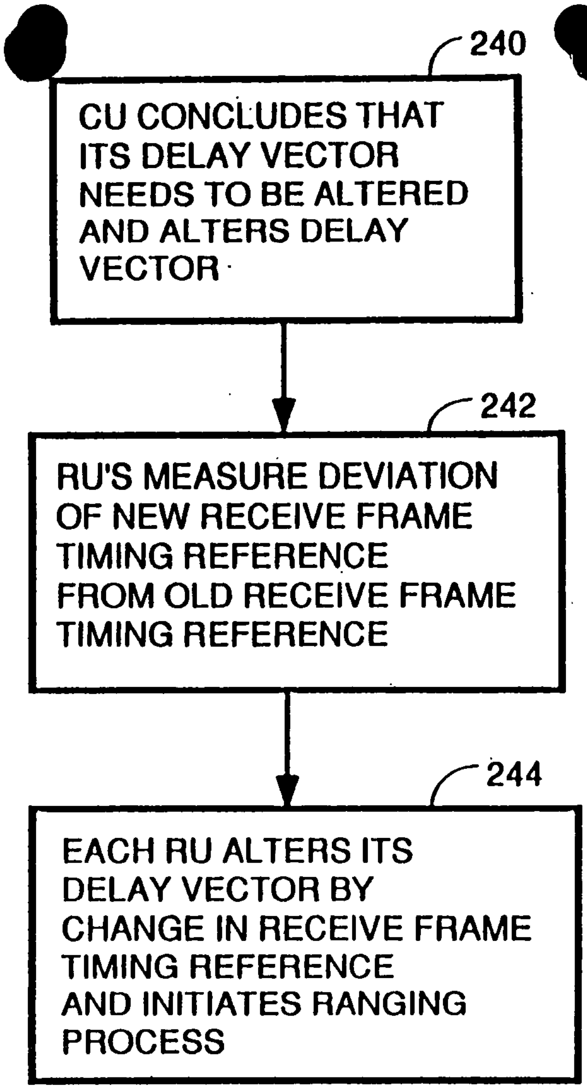

240
CU CONCLUDES THAT ITS DELAY VECTOR NEEDS TO BE ALTERED AND ALTERS DELAY VECTOR
242
RU'S MEASURE DEVIATION OF NEW RECEIVE FRAME TIMING REFERENCE FROM OLD RECEIVE FRAME TIMING REFERENCE
244
EACH RU ALTERS ITS DELAY VECTOR BY CHANGE IN RECEIVE FRAME TIMING REFERENCE AND INITIATES RANGING PROCESS

FIG. ~~8~~ 6

DEAD RECKONING RE-SYNC

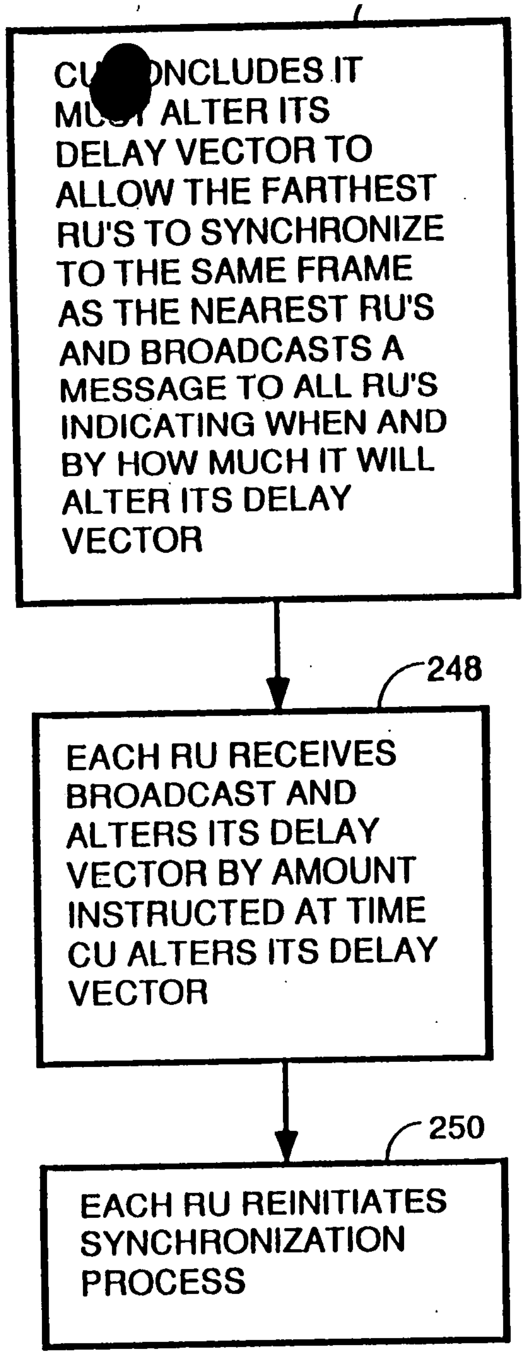
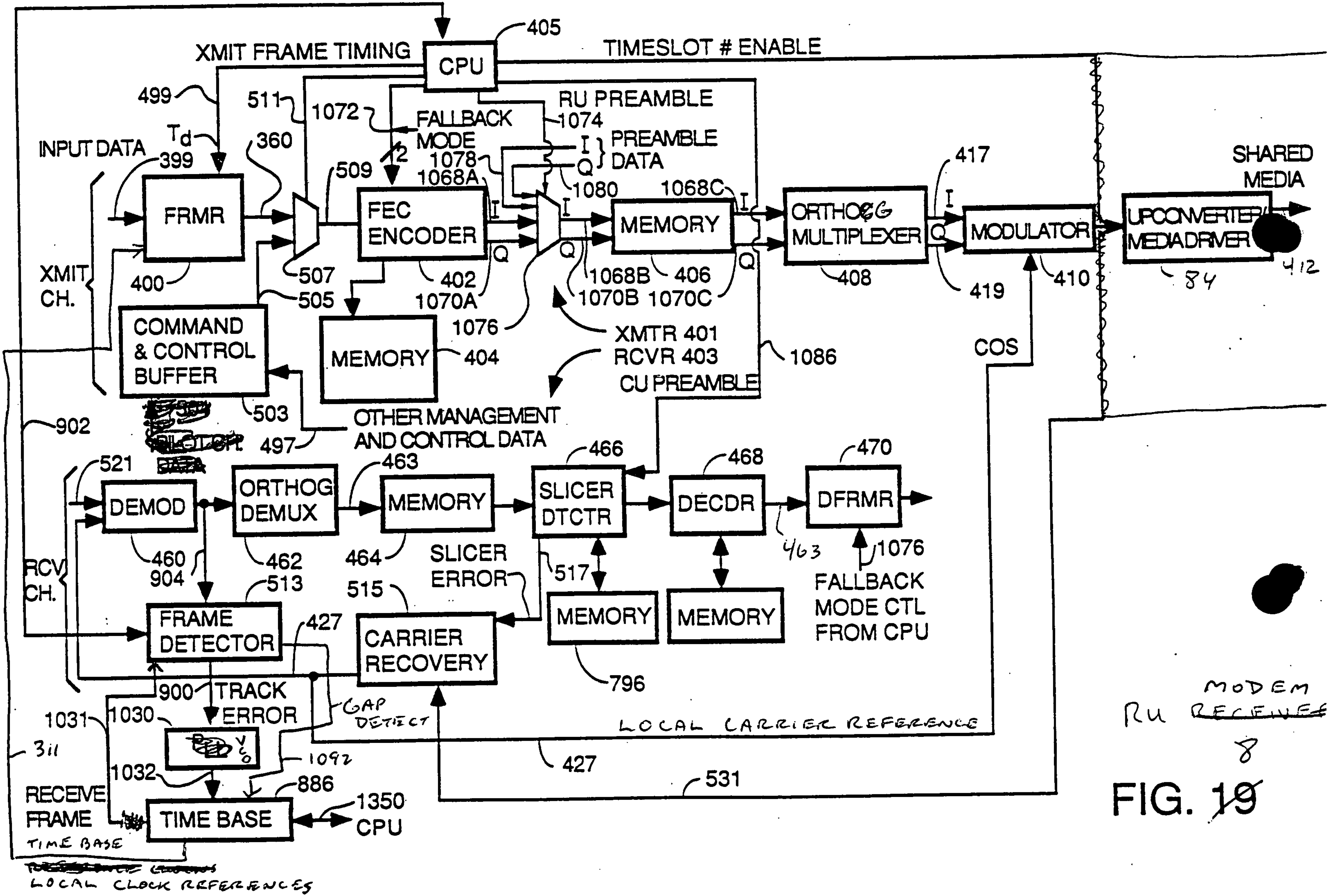

CU CONCLUDES IT MUST ALTER ITS DELAY VECTOR TO ALLOW THE FARTHEST RU'S TO SYNCHRONIZE TO THE SAME FRAME AS THE NEAREST RU'S AND BROADCASTS A MESSAGE TO ALL RU'S INDICATING WHEN AND BY HOW MUCH IT WILL ALTER ITS DELAY VECTOR
248
EACH RU RECEIVES BROADCAST AND ALTERS ITS DELAY VECTOR BY AMOUNT INSTRUCTED AT TIME CU ALTERS ITS DELAY VECTOR
250
EACH RU REINITIATES SYNCHRONIZATION PROCESS

FIG. ~~9~~ 7

PRECURSOR EMBODIMENT

RU

DIGITAL MODEM BLOCK DIAGRAM



XMIT FRAME TIMING
CPU
405
TIMESLOT # ENABLE
499
511
1072
FALLBACK MODE
2
1078
1068A
RU PREAMBLE
1074
I
Q
PREAMBLE DATA
1080
INPUT DATA
Td
399
360
FRMR
509
FEC ENCODER
I
Q
1068C
MEMORY
I
Q
ORTHOGG MULTIPLEXER
417
I
Q
MODULATOR
UPCONVERTER/ MEDIADRIVER
SHARED MEDIA
412
84
XMIT CH.
400
507
505
402
1070A
1068B
406
1070B
1070C
408
419
410
COMMAND & CONTROL BUFFER
MEMORY
404
1076
XMTR 401
RCVR 403
CU PREAMBLE
1086
COS
503
497
OTHER MANAGEMENT AND CONTROL DATA
902
521
DEMOD
ORTHOG DEMUX
463
MEMORY
466
SLICER DTCTR
468
DECDR
470
DFRMR
460
904
462
464
SLICER ERROR
517
463
1076
FALLBACK MODE CTL FROM CPU
RCV CH.
513
515
FRAME DETECTOR
427
CARRIER RECOVERY
MEMORY
MEMORY
796
900
TRACK ERROR
GAP DETECT
1031
1030
VCO
LOCAL CARRIER REFERENCE
311
1032
1092
427
531
886
RECEIVE FRAME
TIME BASE
1350
CPU
TIME BASE
~~LOCAL CLOCKS~~
LOCAL CLOCK REFERENCES

MODEM

RU ~~RECEIVER~~

8

FIG. ~~19~~

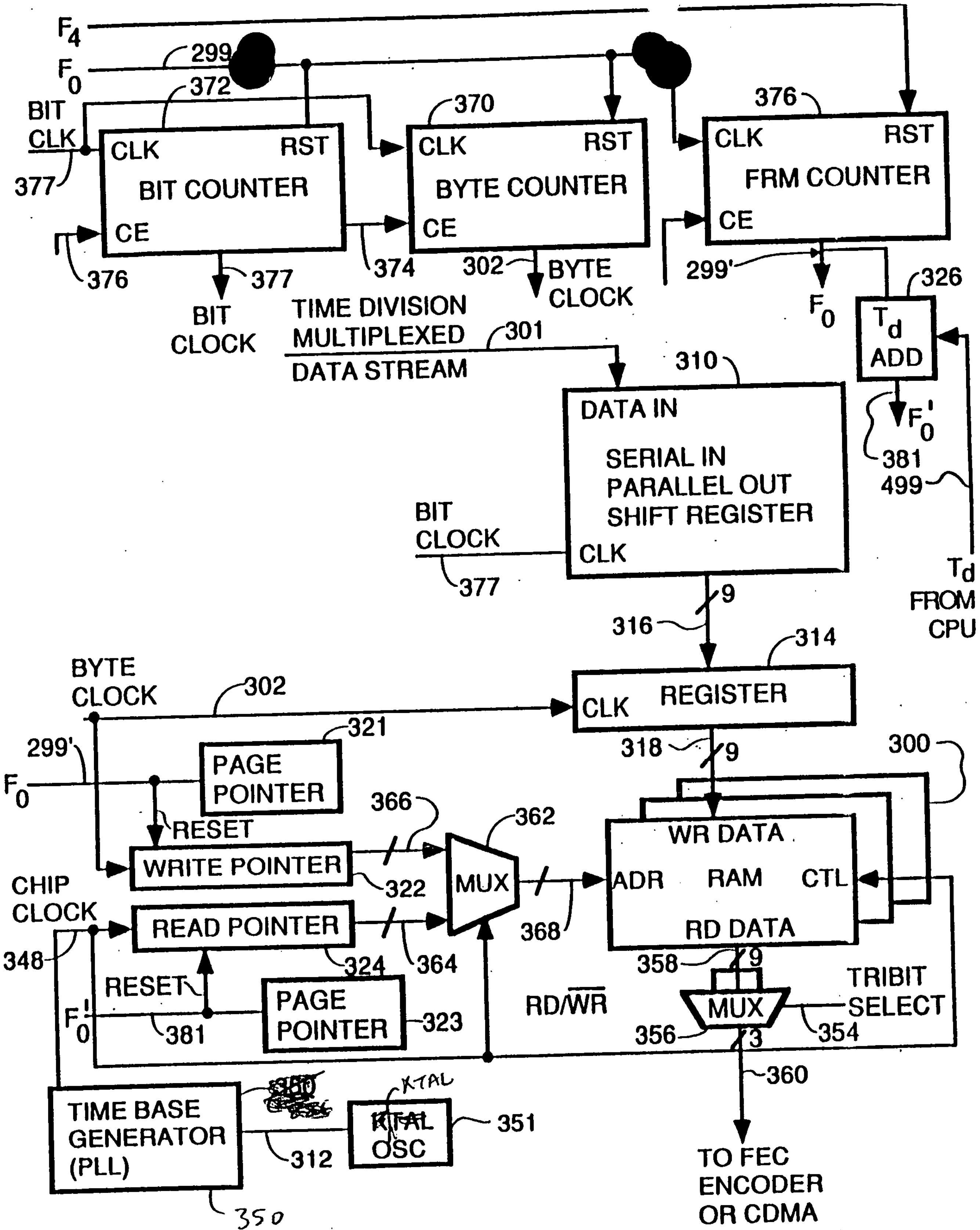

F4
F0
299
372
BIT CLK
377
376
CLK
RST
BIT COUNTER
CE
377
BIT CLOCK
374
370
BYTE COUNTER
302
BYTE CLOCK
376
FRM COUNTER
299'
F0
326
Td ADD
F0'
381
499
Td FROM CPU
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
BIT CLOCK
377
9
316
314
REGISTER
BYTE CLOCK
302
318
9
300
299'
F0
321
PAGE POINTER
RESET
WRITE POINTER
366
362
MUX
322
CHIP CLOCK
348
READ POINTER
324
364
368
RESET
F0'
381
PAGE POINTER
323
WR DATA
ADR
RAM
CTL
RD DATA
358
9
RD/$\overline{WR}$
MUX
356
3
TRIBIT SELECT
354
360
TO FEC ENCODER OR CDMA MUX/BUFFER
TIME BASE GENERATOR (PLL)
~~350~~
XTAL
~~XTAL~~ OSC
351
312
350

FIG. ~~12~~ 9

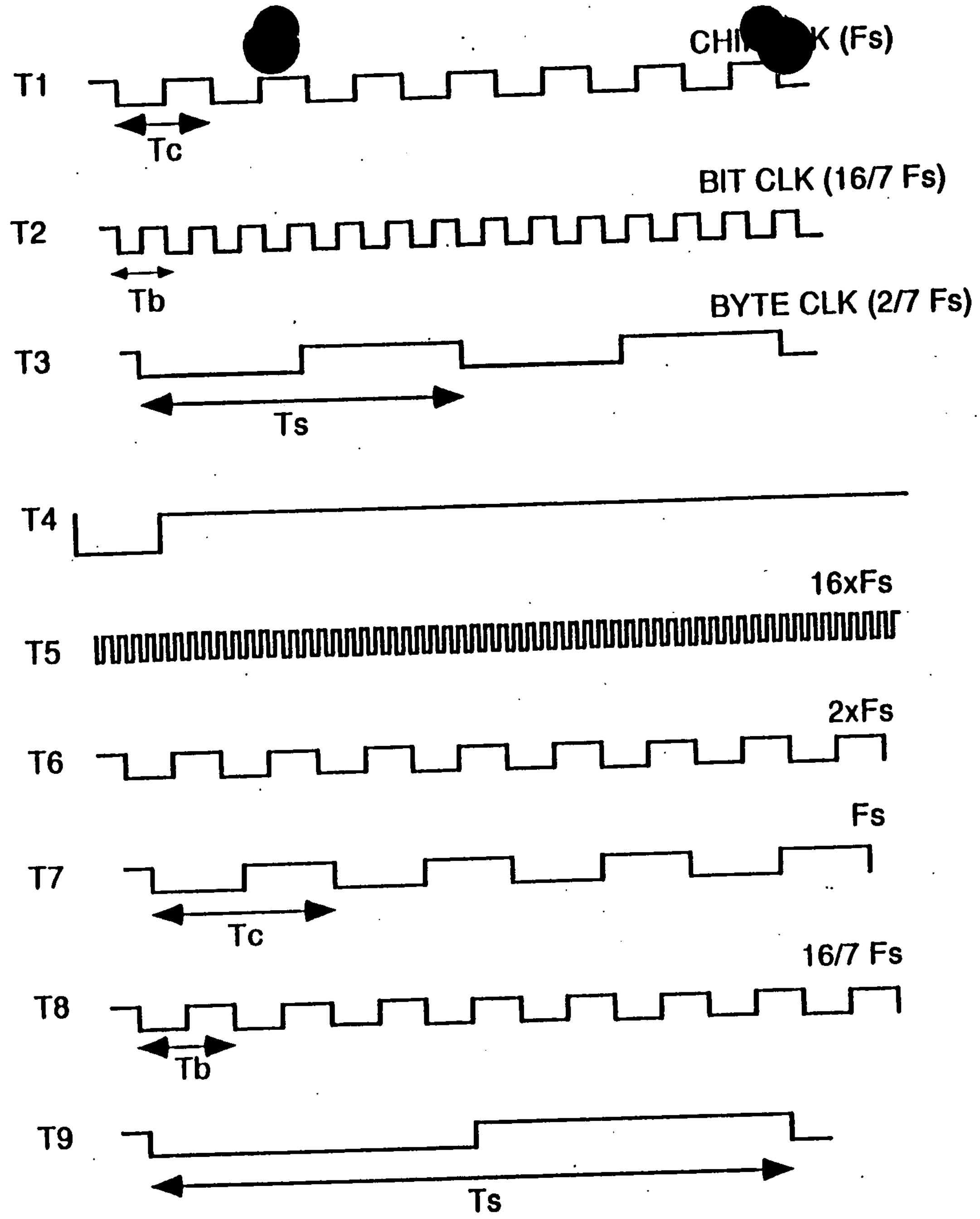

CHI[illegible]K (Fs)
T1
Tc
BIT CLK (16/7 Fs)
T2
Tb
BYTE CLK (2/7 Fs)
T3
Ts
T4
16xFs
T5
2xFs
T6
Fs
T7
Tc
16/7 Fs
T8
Tb
T9
Ts

FIG. ~~13~~ 10

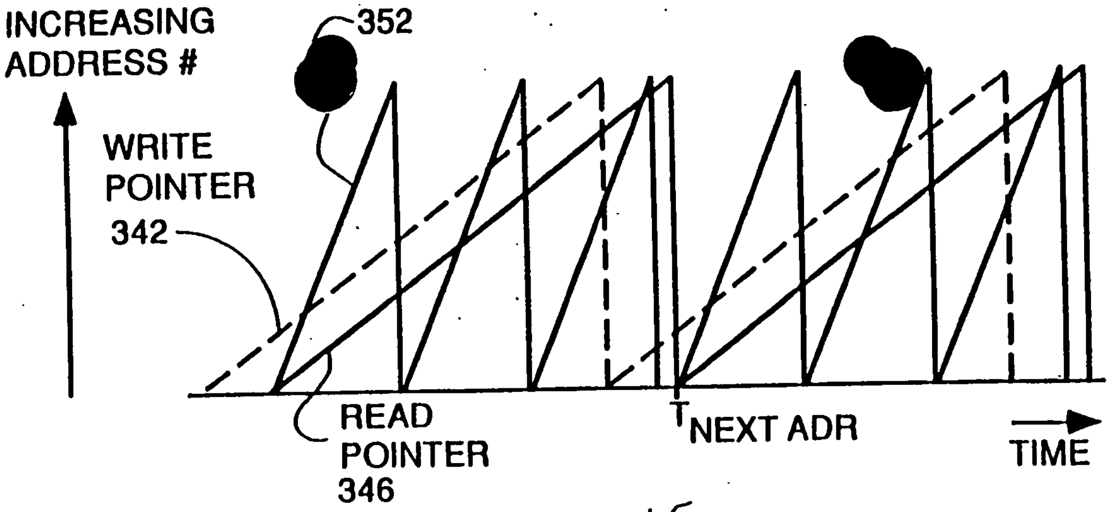


FIG. ~~17~~ 15

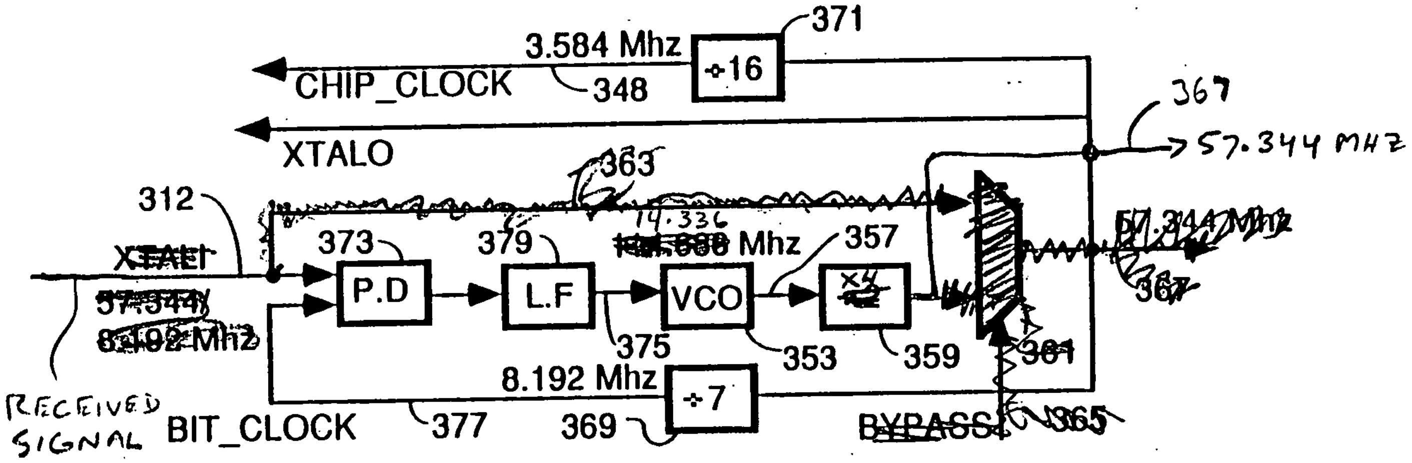

371
3.584 Mhz
÷16
CHIP_CLOCK
348
367
XTALO
57.344 MHZ
363
312
~~XTALI~~
~~57.344/~~
~~8.192 Mhz~~
373
P.D
379
L.F
14.336
~~14.336~~ Mhz
VCO
357
×4
~~57.344 Mhz~~
~~367~~
375
353
359
~~361~~
8.192 Mhz
÷7
RECEIVED SIGNAL
BIT_CLOCK
377
369
~~BYPASS~~
~~365~~

FIG. ~~18~~ 11

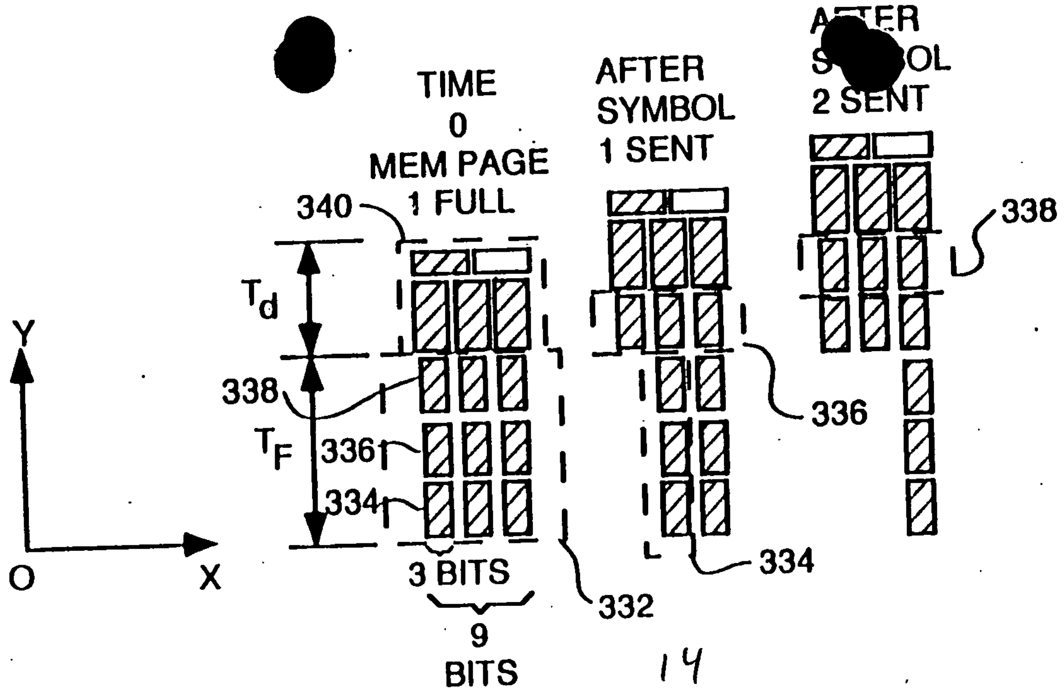

TIME
0
MEM PAGE
1 FULL
AFTER
SYMBOL
1 SENT
A[illegible]ER
S[illegible]OL
2 SENT
340
338
338
Td
TF
336
334
336
334
Y
O
X
3 BITS
9
BITS
332

FIG. ~~14~~ 14 ok

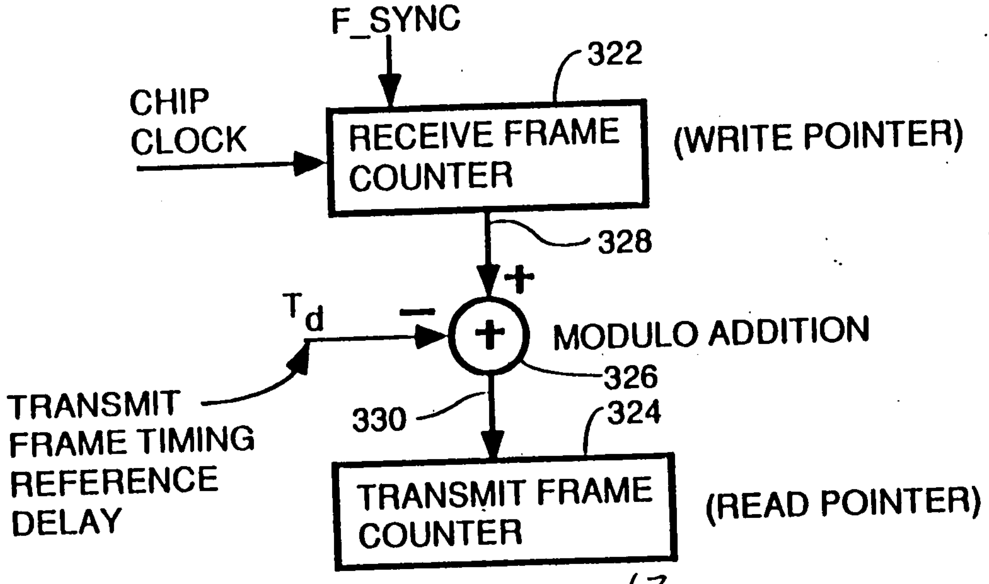

F_SYNC
322
CHIP
CLOCK
RECEIVE FRAME
COUNTER
(WRITE POINTER)
328
+
−
Td
MODULO ADDITION
326
TRANSMIT
FRAME TIMING
REFERENCE
DELAY
330
324
TRANSMIT FRAME
COUNTER
(READ POINTER)

FIG. ~~15~~ 12

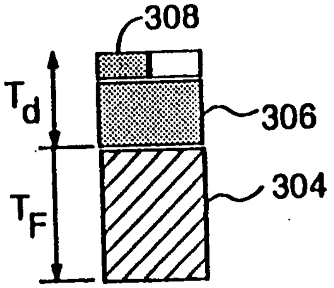

308
Td
306
TF
304

FIG. ~~16~~ 13

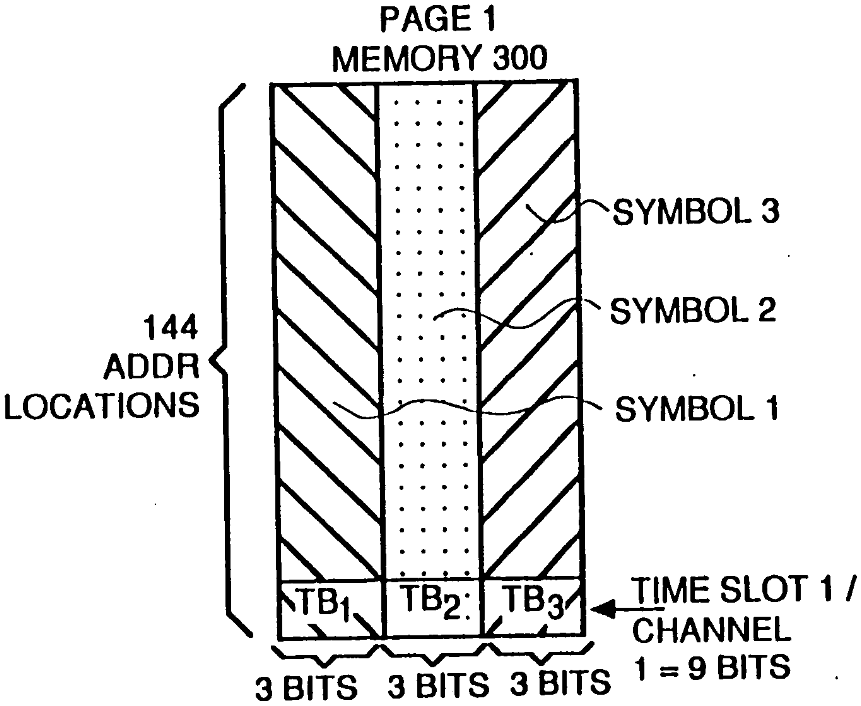
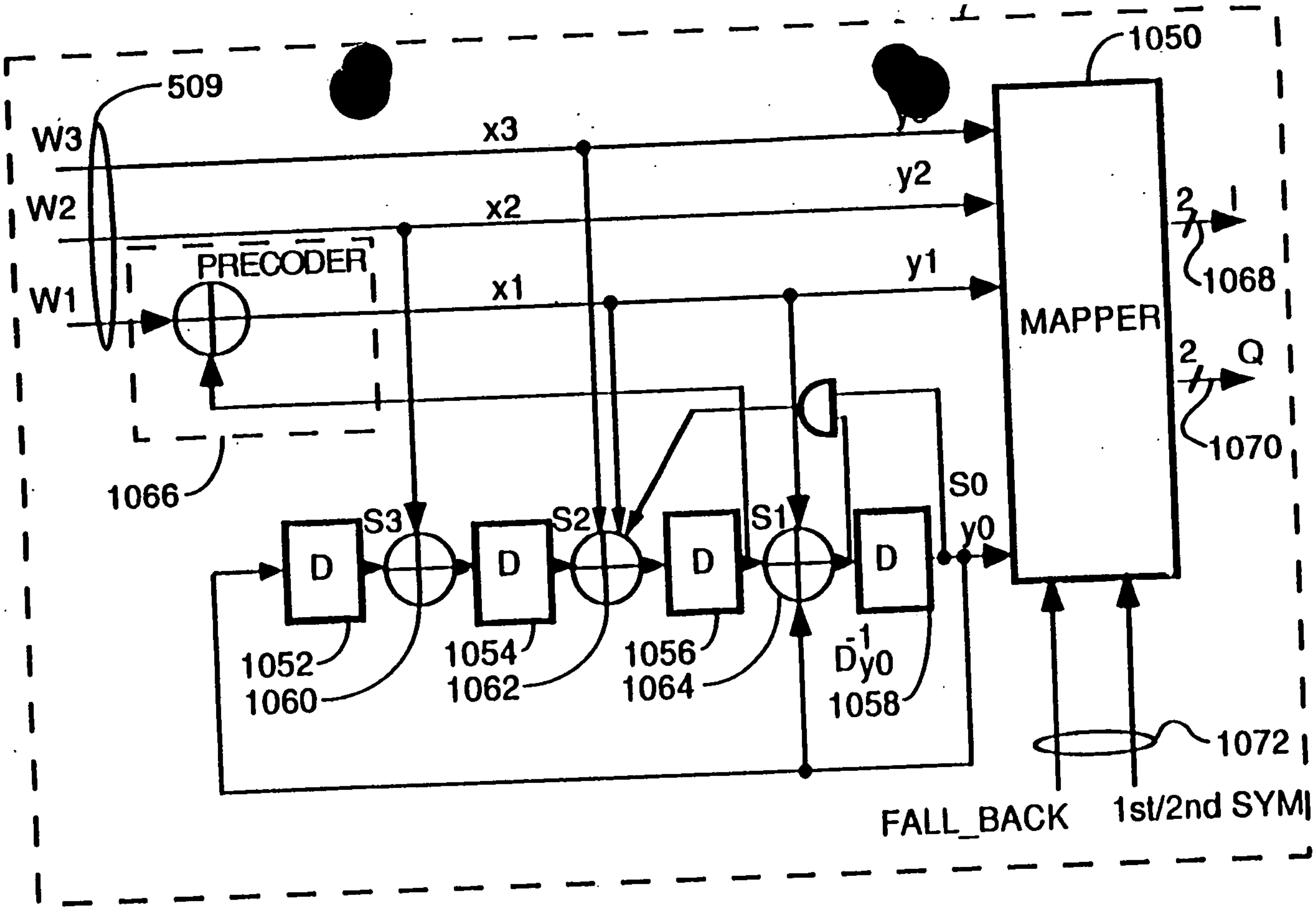

PAGE 1
MEMORY 300
SYMBOL 3
SYMBOL 2
SYMBOL 1
144
ADDR
LOCATIONS
TB_1
TB_2
TB_3
TIME SLOT 1 / CHANNEL 1 = 9 BITS
3 BITS
3 BITS
3 BITS

FIG. ~~20~~ 16


509
W3
W2
W1
x3
y2
x2
PRECODER
x1
y1
1050
MAPPER
2
I
1068
2
Q
1070
1066
S3
S2
S1
S0
y0
D
D
D
D
1052
1060
1054
1062
1056
1064
$D^{-1}y0$
1058
1072
FALL_BACK
1st/2nd SYM

PREFERRED TRELLIS ENCODER

FIG. ~~42~~ 17

MAPPING FOR FALL-BACK MODE - LSB'S

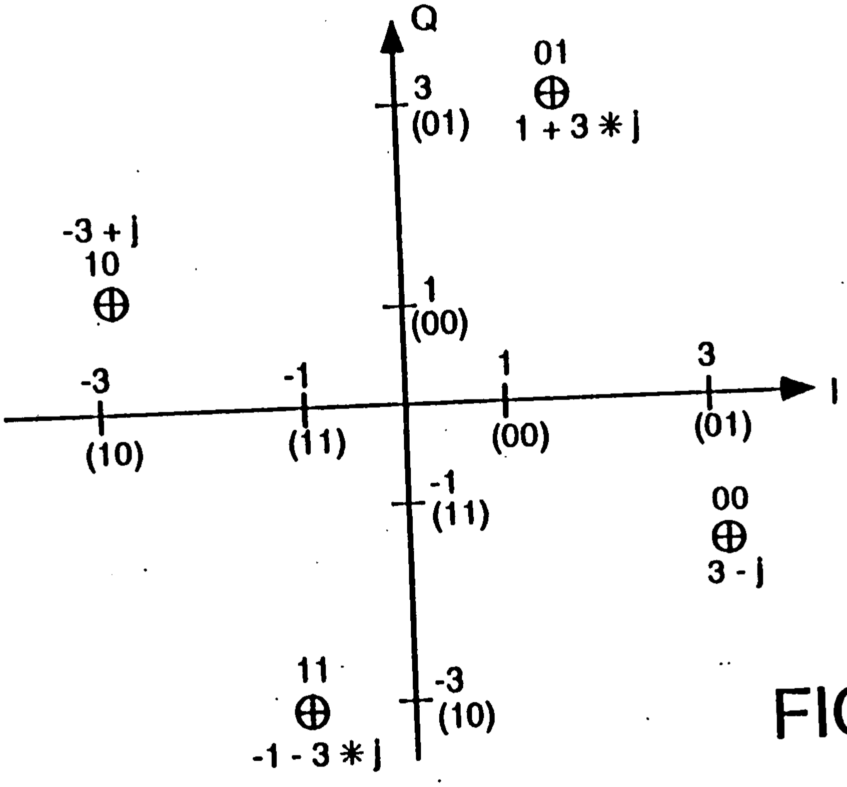

Q
3
(01)
01
1 + 3 * j
-3 + j
10
1
(00)
-3
(10)
-1
(11)
1
(00)
3
(01)
I
-1
(11)
00
3 - j
11
-1 - 3 * j
-3
(10)

FIG. ~~43~~ 21

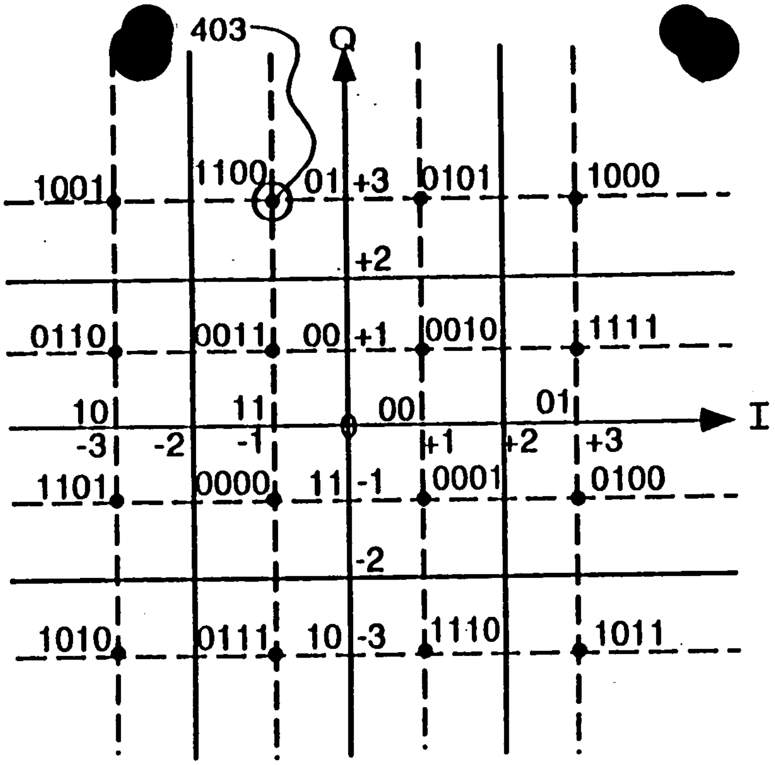
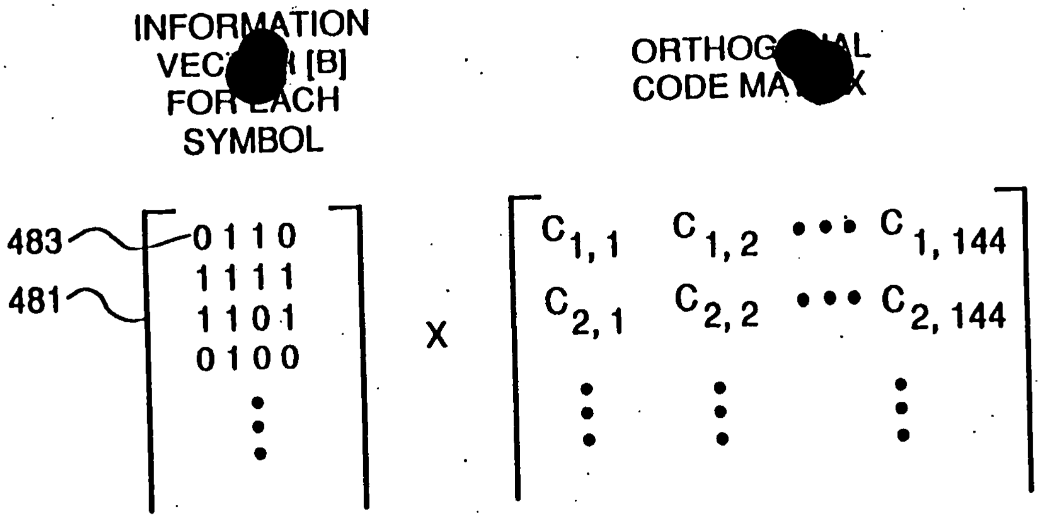

403
Q
I
1001
1100
01
+3
0101
1000
+2
0110
0011
00
+1
0010
1111
10
11
00
01
-3
-2
-1
0
+1
+2
+3
1101
0000
11
-1
0001
0100
-2
1010
0111
10
-3
1110
1011

FIG. ~~21~~ 18

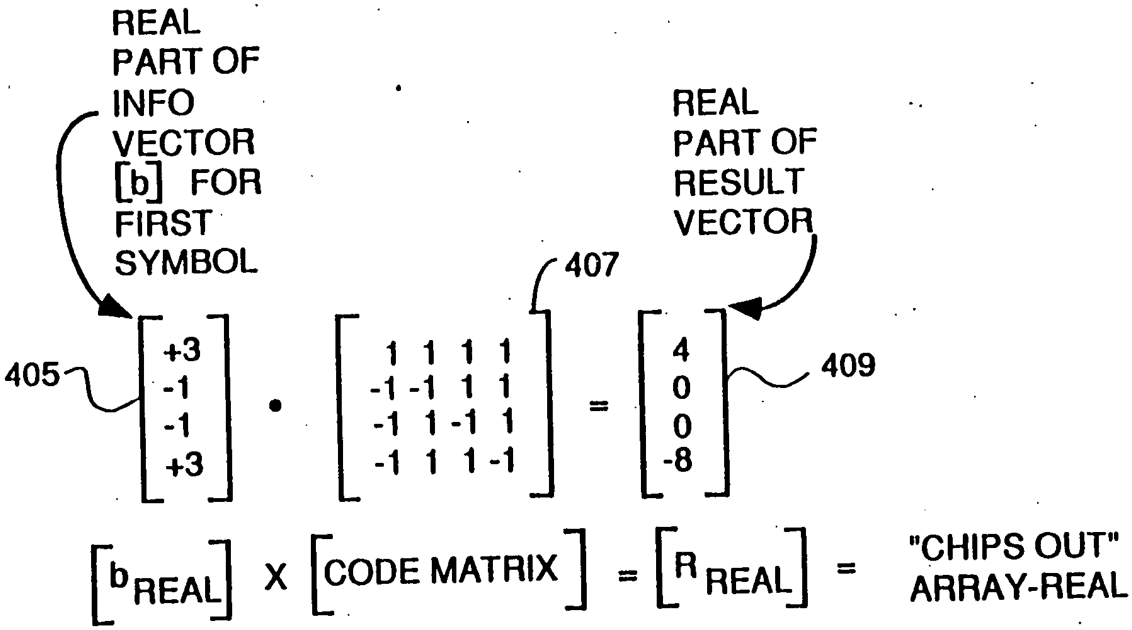
CODE	INPHASE	QUADRATURE	
0000	111	111	= -1 -
0001	001	111	= 1 - j
0010	001	001	= 1+ j
0011	111	001	= -1+ j
0100	011	111	= 3 - j
0101	001	011	= 1+ 3∗j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3∗ j
1000	011	011	=+3 + 3∗j
1001	101	011	= -3 + 3∗j
1010	101	101	= -3 - 3∗ j
1011	011	101	= 3 - 3∗ j
403 1100	111	011	= -1+ 3∗ j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3∗ j
1111	011	001	= 3 + j

FIG. ~~22~~ 19


INFORMATION
VEC[illegible]R [B]
FOR EACH
SYMBOL
ORTHOG[illegible]AL
CODE MA[illegible]X
483
481
0 1 1 0
1 1 1 1
1 1 0 1
0 1 0 0
X
C1,1 C1,2 C1,144
C2,1 C2,2 C2,144

20 A

FIG. ~~23~~A


REAL
PART OF
INFO
VECTOR
[b] FOR
FIRST
SYMBOL
REAL
PART OF
RESULT
VECTOR
407
405
409
+3
-1
-1
+3
1 1 1 1
-1 -1 1 1
-1 1 -1 1
-1 1 1 -1
=
4
0
0
-8
[bREAL] X [CODE MATRIX] = [RREAL] = "CHIPS OUT" ARRAY-REAL

20 B

FIG. ~~23~~B

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. ~~44~~ 22

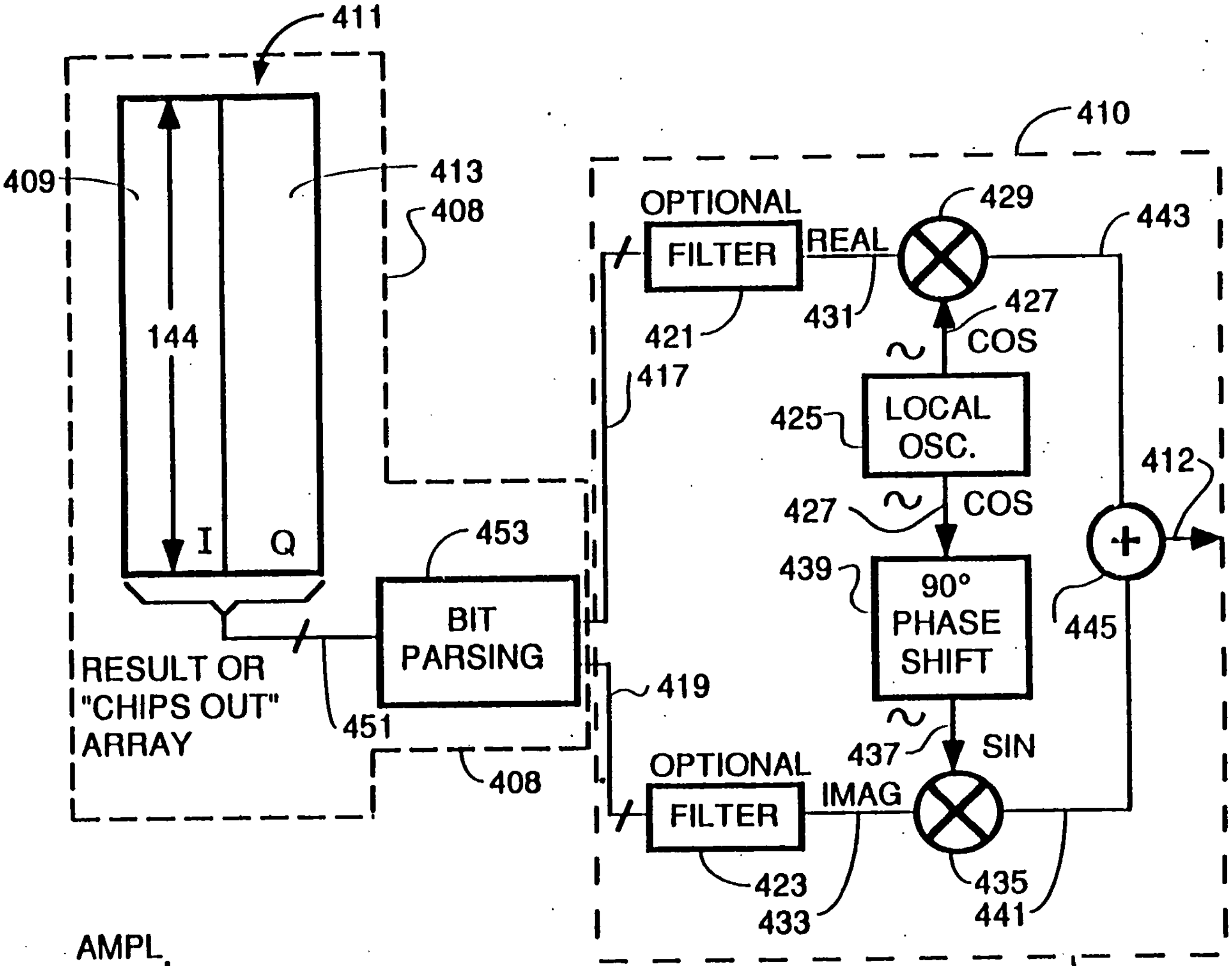

411
409
413
408
144
I
Q
RESULT OR "CHIPS OUT" ARRAY
451
453
BIT PARSING
408
410
OPTIONAL FILTER
REAL
429
443
421
431
427
COS
417
LOCAL OSC.
425
427
COS
412
439
90° PHASE SHIFT
445
419
437
SIN
OPTIONAL FILTER
IMAG
423
433
435
441
410

FIG. ~~24~~ 23

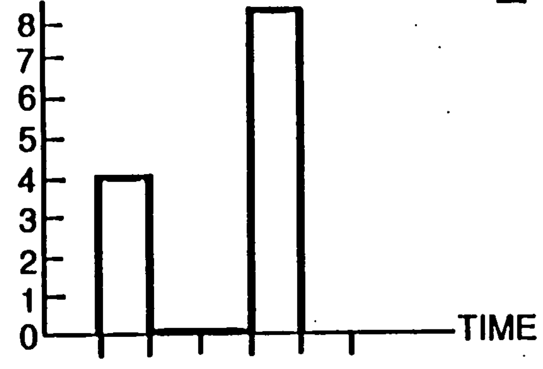
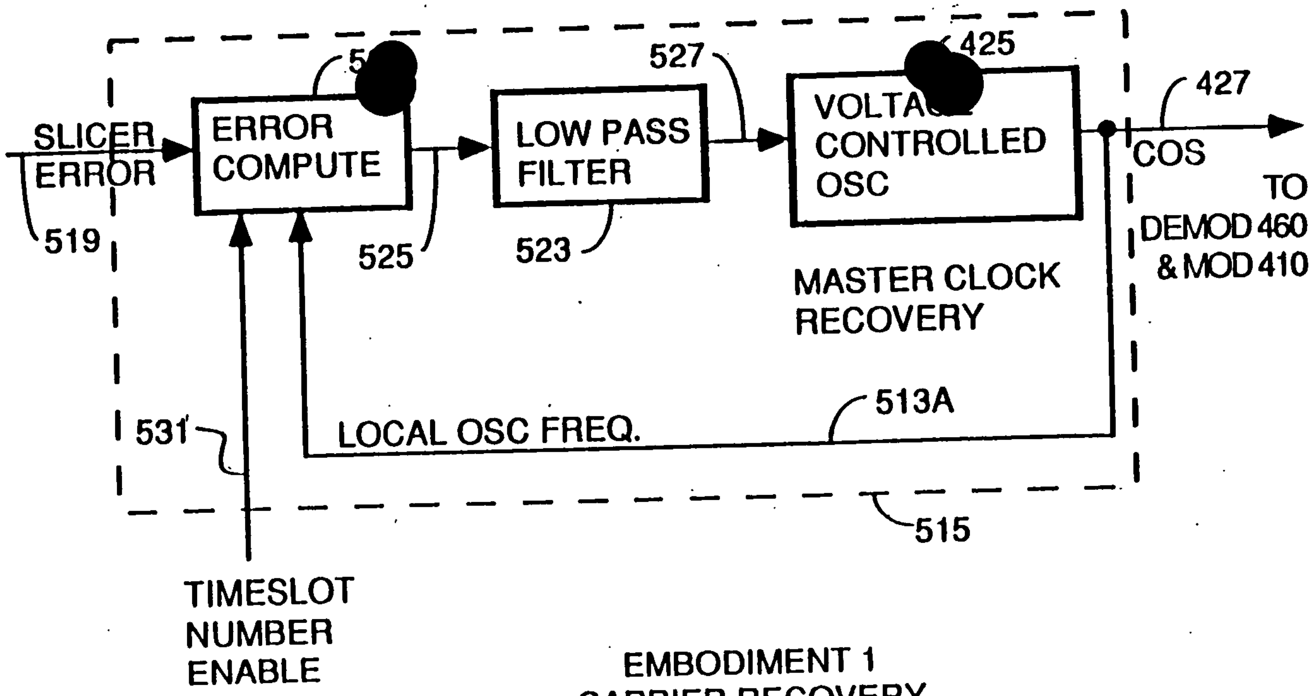


FIG. ~~25~~ 24

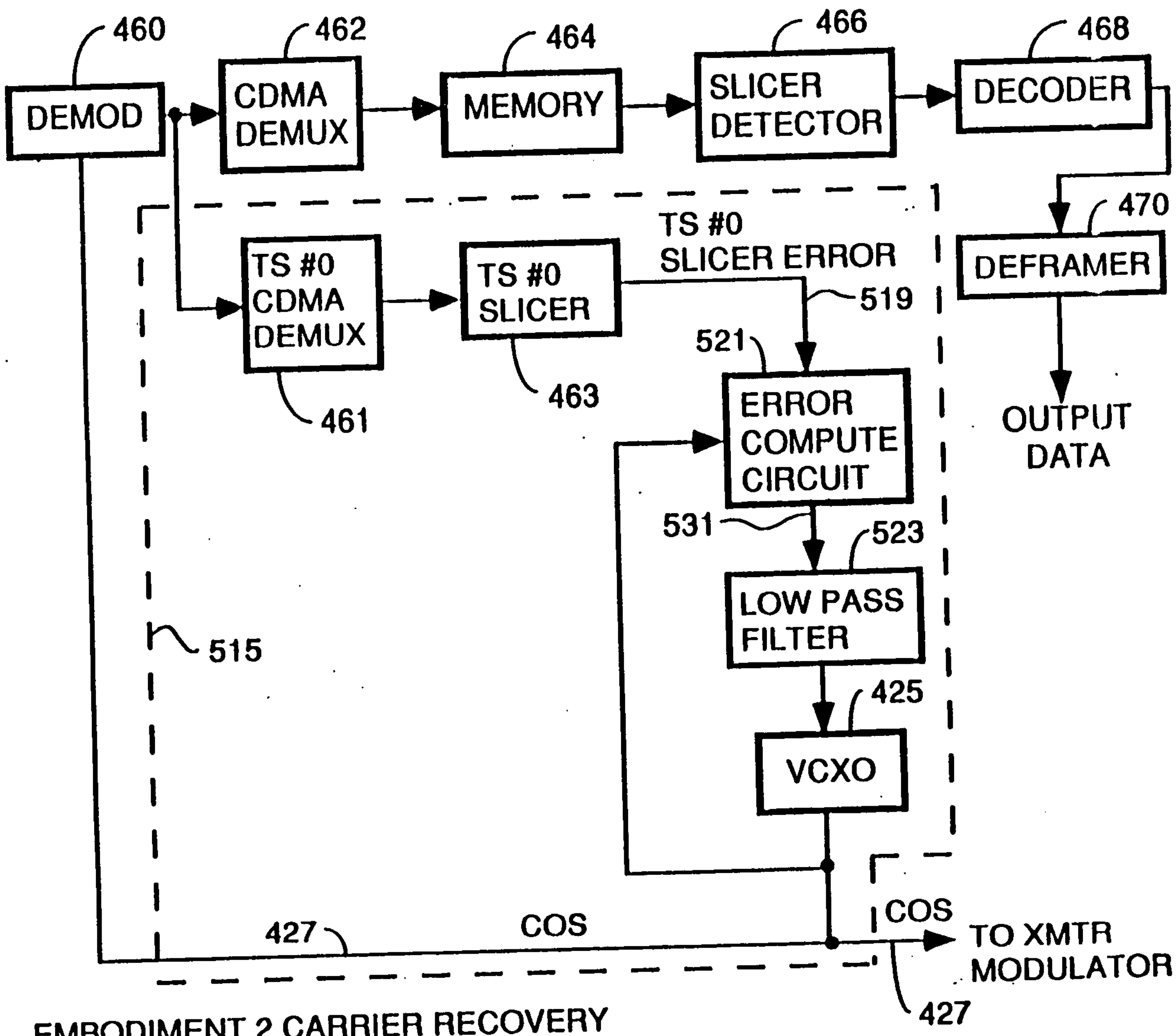


SLICER ERROR
519
ERROR COMPUTE
5
525
LOW PASS FILTER
523
527
VOLTA CONTROLLED OSC
425
427
COS
TO DEMOD 460. & MOD 410
MASTER CLOCK RECOVERY
LOCAL OSC FREQ.
513A
531
515
TIMESLOT NUMBER ENABLE

EMBODIMENT 1 CARRIER RECOVERY

FIG. ~~35~~

25



460
DEMOD
462
CDMA DEMUX
464
MEMORY
466
SLICER DETECTOR
468
DECODER
470
DEFRAMER
OUTPUT DATA
TS #0 CDMA DEMUX
461
TS #0 SLICER
463
TS #0 SLICER ERROR
519
521
ERROR COMPUTE CIRCUIT
531
523
LOW PASS FILTER
425
VCXO
515
427
COS
COS
TO XMTR MODULATOR
427

EMBODIMENT 2 CARRIER RECOVERY

FIG. ~~36~~

26

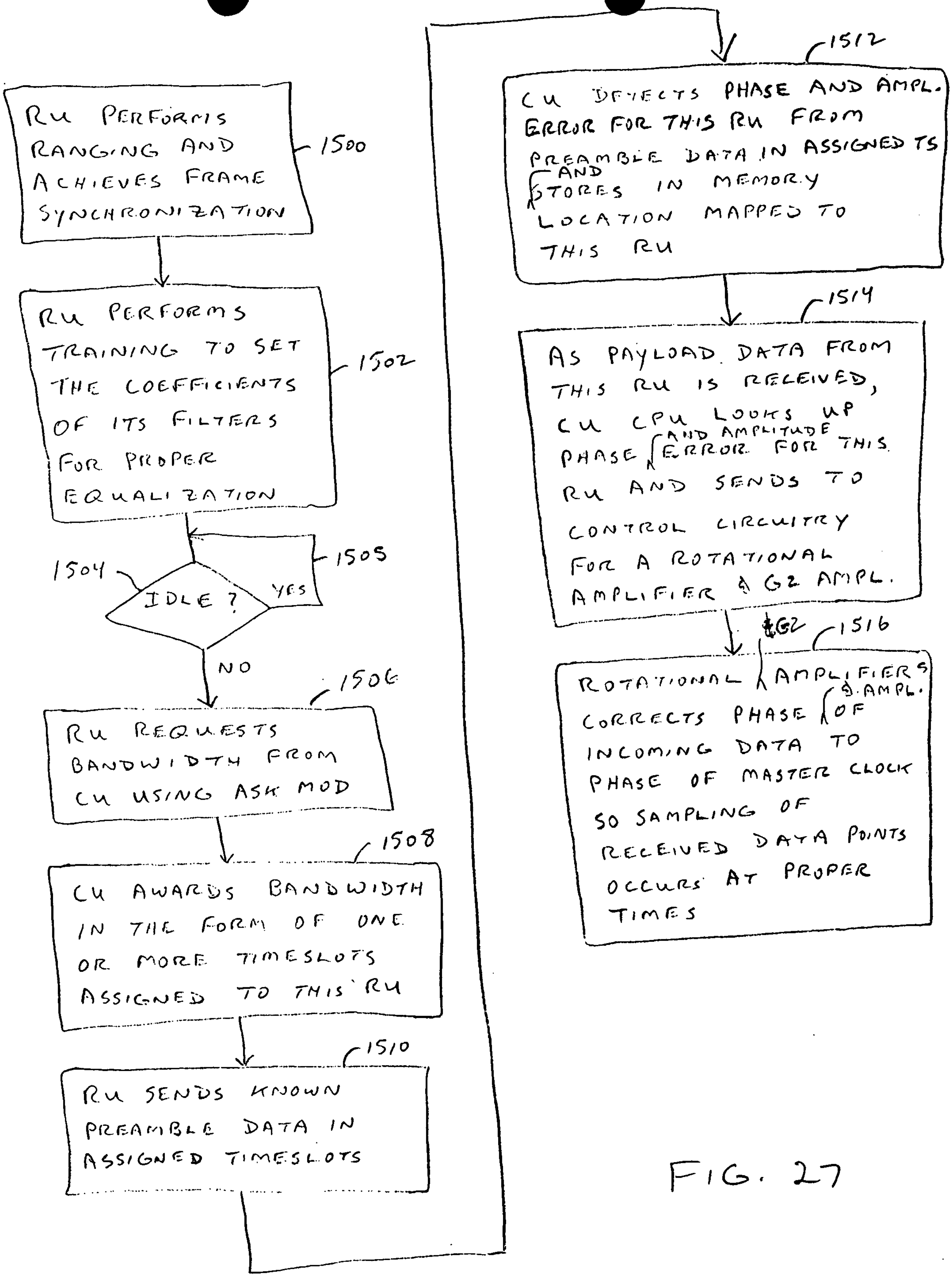
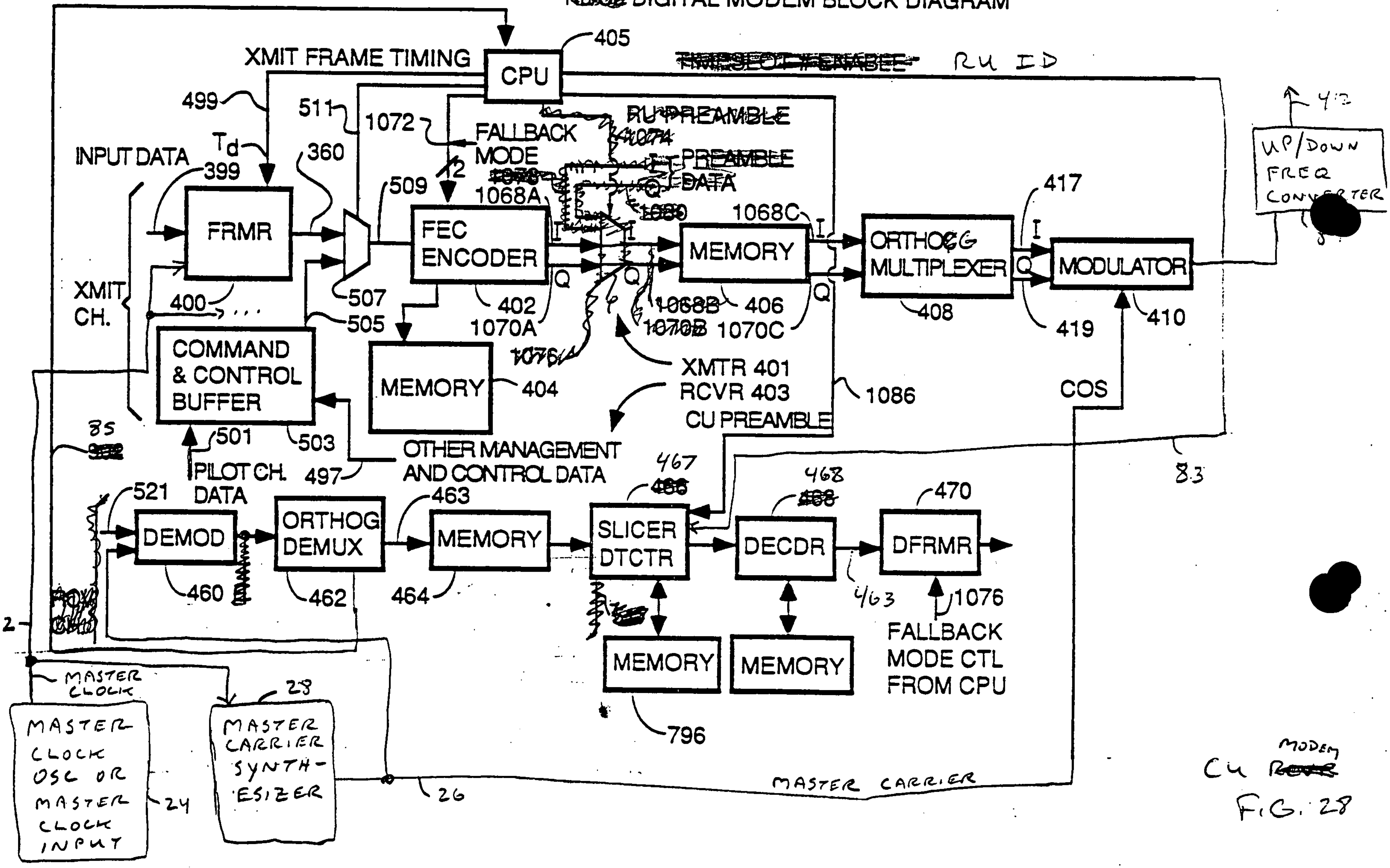

RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1500
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1502
1504
IDLE ?
YES
1505
NO
1506
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1508
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1510
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1512
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED TS AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1514
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1516
ROTATIONAL & G2 AMPLIFIERS CORRECTS PHASE & AMPL. OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES

FIG. 27

CU

~~RU~~ DIGITAL MODEM BLOCK DIAGRAM



~~TIMESLOT ENABLE~~
RU ID
XMIT FRAME TIMING
CPU
405
499
511
1072
FALLBACK MODE
12
~~1078~~
1068A
~~RU PREAMBLE~~
~~1074~~
~~PREAMBLE~~
~~DATA~~
~~1080~~
INPUT DATA
Td
399
360
FRMR
509
FEC ENCODER
I
Q
1068C
MEMORY
I
Q
ORTHOG MULTIPLEXER
417
I
Q
MODULATOR
UP/DOWN FREQ CONVERTER
42
XMIT CH.
400
507
505
402
1070A
~~1068B~~
406
~~1070B~~
1070C
408
419
410
COMMAND & CONTROL BUFFER
~~1076~~
MEMORY
404
XMTR 401
RCVR 403
CU PREAMBLE
1086
COS
85
~~332~~
501
503
PILOT CH. DATA
497
OTHER MANAGEMENT AND CONTROL DATA
467
~~466~~
468
~~468~~
470
83
521
DEMOD
ORTHOG DEMUX
463
MEMORY
SLICER DTCTR
DECDR
DFRMR
460
462
464
463
1076
FALLBACK MODE CTL FROM CPU
2
MEMORY
MEMORY
796
MASTER CLOCK
28
MASTER CLOCK OSC OR MASTER CLOCK INPUT
24
MASTER CARRIER SYNTH-ESIZER
26
MASTER CARRIER

CU MODEM ~~RU~~

FIG. 28

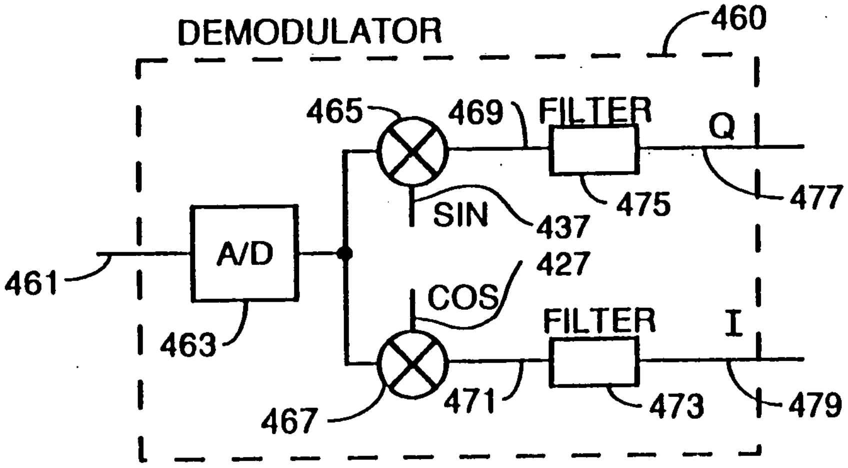
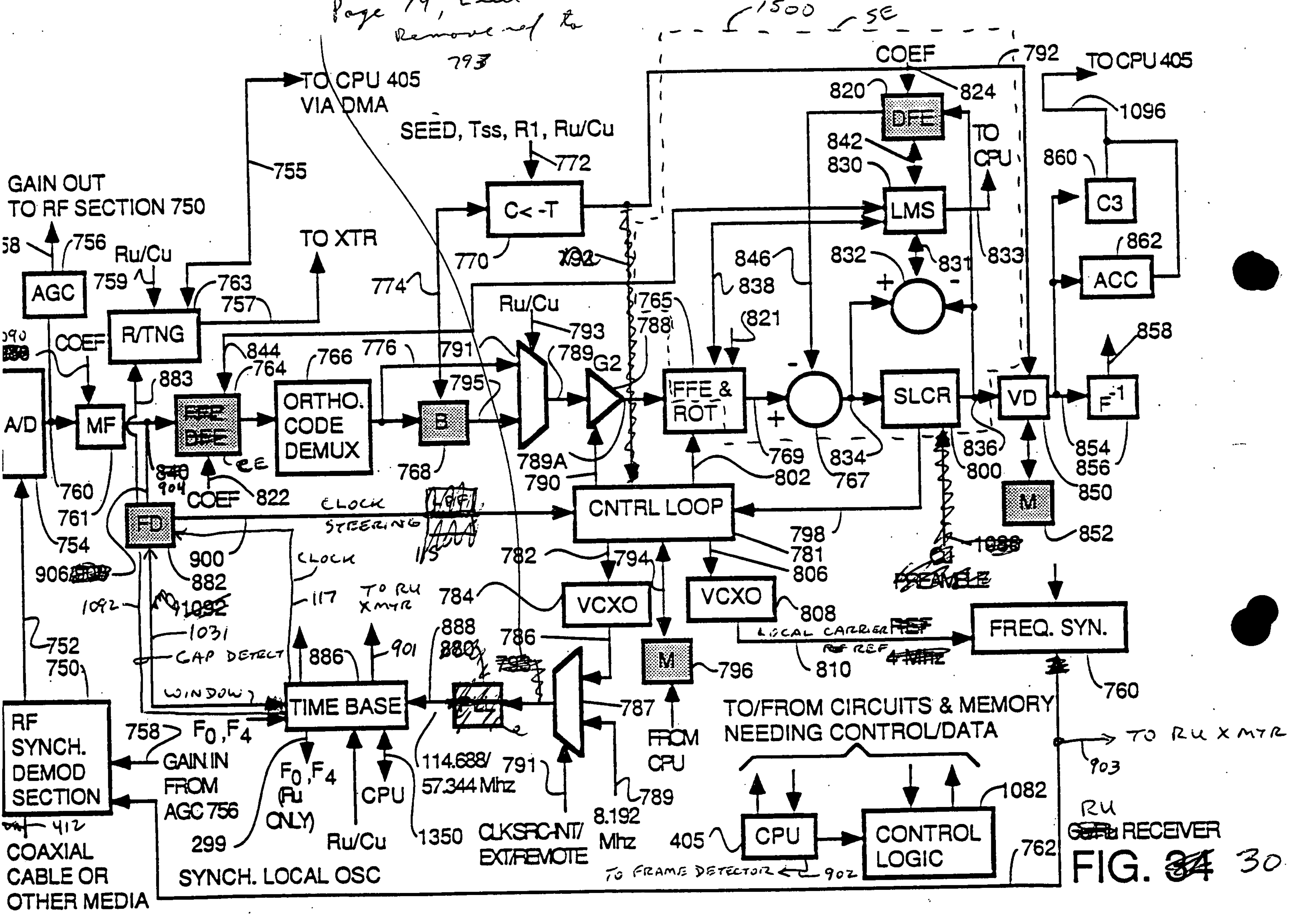

DEMODULATOR
FILTER
Q
SIN
A/D
COS
FILTER
I

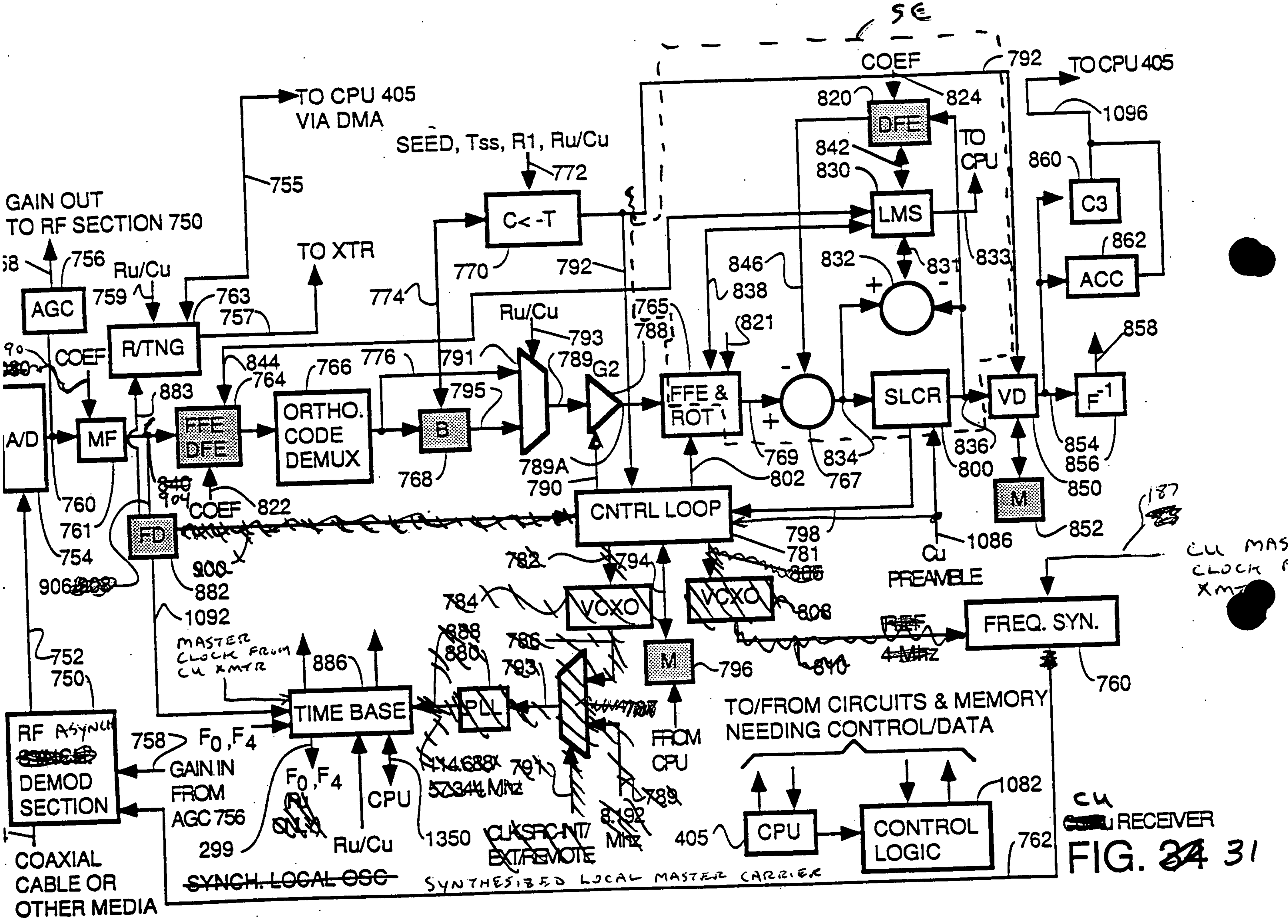
FIG. ~~26~~ 29

Page 94, Line 8
Removed ref to
793


1500
SE
TO CPU 405
VIA DMA
755
SEED, Tss, R1, Ru/Cu
772
C< -T
770
774
COEF
792
824
820
DFE
842
830
LMS
TO CPU
833
TO CPU 405
1096
860
C3
862
ACC
858
F^-1
GAIN OUT
TO RF SECTION 750
58
756
AGC
Ru/Cu
759
R/TNG
763
757
TO XTR
~~X92~~
765
788
846
838
821
832
831
COEF
090
A/D
MF
883
~~FFE~~ DFE
844
764
766
ORTHO. CODE DEMUX
776
791
795
B
Ru/Cu
793
789
G2
FFE & ROT
SLCR
VD
854
856
850
836
800
769
802
834
767
M
852
760
761
754
~~840~~
904
CE
COEF
822
768
789A
790
FD
CLOCK STEERING
LPF
1/S
CNTRL LOOP
798
781
806
~~1088~~
~~PREAMBLE~~
900
882
906
782
794
CLOCK
117
1092
~~1092~~
1031
CAP DETECT
TO RU XMTR
784
VCXO
VCXO
808
LOCAL CARRIER ~~REF~~
~~RF~~ REF ~~4 MHz~~
810
FREQ. SYN.
760
752
750
WINDOW
888
~~880~~
786
~~793~~
M
796
901
886
TIME BASE
787
FROM CPU
TO/FROM CIRCUITS & MEMORY NEEDING CONTROL/DATA
TO RU XMTR
903
RF SYNCH. DEMOD SECTION
758
F0, F4
GAIN IN FROM AGC 756
F0, F4 (Ru ONLY)
CPU
114.688/57.344 Mhz
791
789
8.192 Mhz
1082
412
COAXIAL CABLE OR OTHER MEDIA
299
SYNCH. LOCAL OSC
Ru/Cu
1350
CLKSRC-INT/EXT/REMOTE
405
CPU
CONTROL LOGIC
762
TO FRAME DETECTOR
902

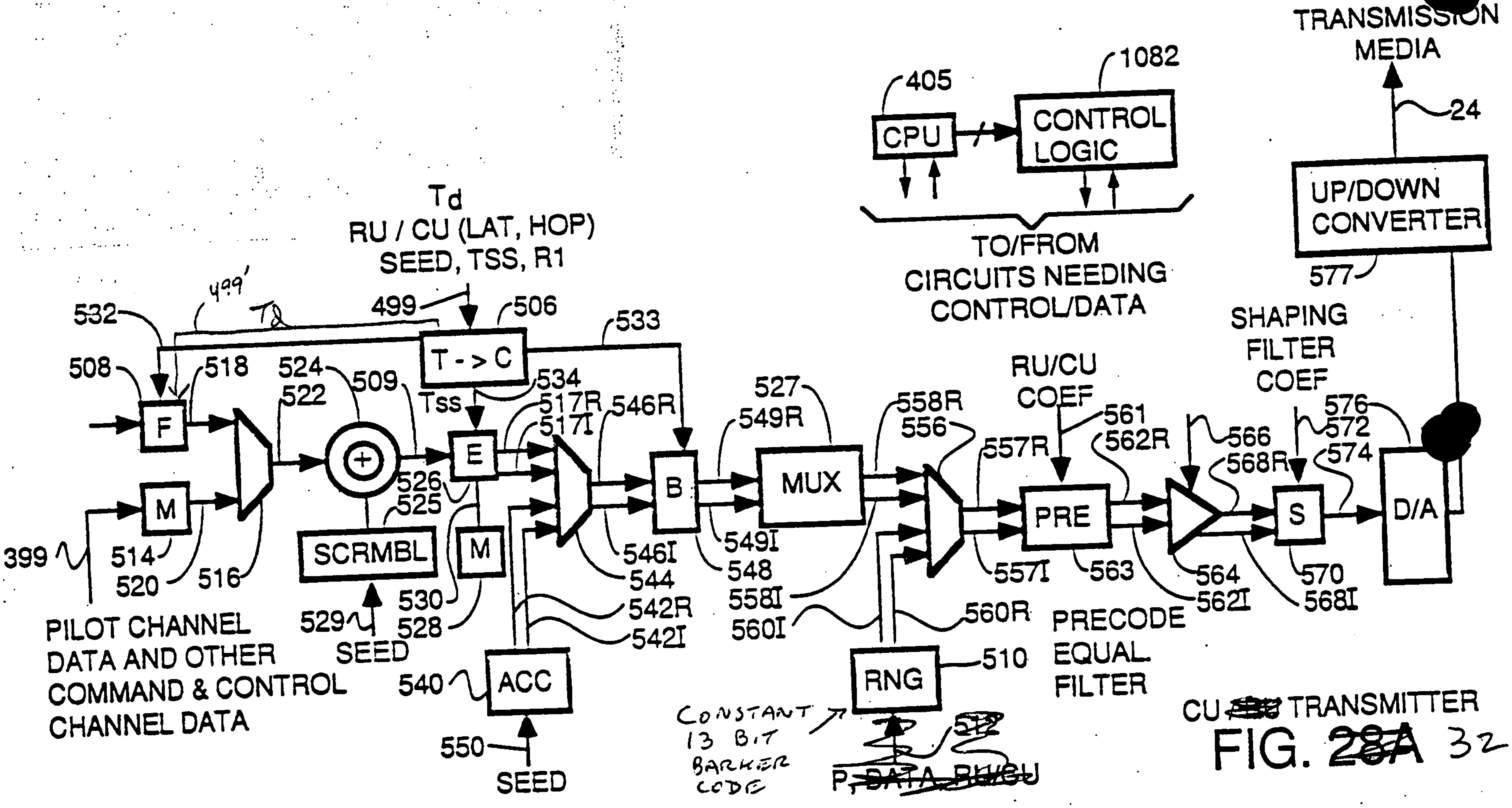
RU ~~Gen~~ RECEIVER

FIG. ~~34~~ 30


SE
COEF
792
TO CPU 405
820
824
DFE
1096
842
830
TO CPU
860
C3
LMS
833
862
ACC
846
838
832
831
821
858
F^-1
VD
SLCR
FFE & ROT
+
-
836
800
854
856
850
769
802
834
767
M
852
CNTRL LOOP
798
781
~~806~~
1086
Cu
PREAMBLE
187
~~185~~
Cu MAST CLOCK FROM XMTR
782
794
VCXO
VCXO
808
784
FREQ. SYN.
~~REF~~
~~4 MHz~~
810
760
TO CPU 405 VIA DMA
SEED, Tss, R1, Ru/Cu
772
755
C<-T
770
792
GAIN OUT TO RF SECTION 750
58
756
AGC
Ru/Cu
759
R/TNG
763
757
TO XTR
774
776
Ru/Cu
793
789
G2
765
788
90
~~80~~
COEF
MF
883
844
764
FFE DFE
766
ORTHO. CODE DEMUX
791
795
B
768
789A
790
A/D
~~840~~
904
COEF
822
760
761
754
906~~808~~
FD
900
882
1092
MASTER CLOCK FROM CU XMTR
752
750
RF ASYNCH ~~SYNCH~~ DEMOD SECTION
758
F0, F4
GAIN IN FROM AGC 756
TIME BASE
886
~~888~~
880
PLL
786
783
~~SIMULATE~~
796
M
FROM CPU
~~114.688~~
~~57.344 MHz~~
791
789
8.192 MHz
F0, F4
(R) ONLY
CPU
Ru/Cu
1350
299
CLKSRC INT/EXT REMOTE
405
TO/FROM CIRCUITS & MEMORY NEEDING CONTROL/DATA
CPU
CONTROL LOGIC
1082
762
COAXIAL CABLE OR OTHER MEDIA
~~SYNCH. LOCAL OSC~~
SYNTHESIZED LOCAL MASTER CARRIER

CU ~~CU~~ RECEIVER

FIG. ~~24~~ 31


Td
RU / CU (LAT, HOP)
SEED, TSS, R1
499'
Td
532
508
F
518
524
522
509
499
506
T - > C
533
534
Tss
E
517R
517I
546R
B
527
549R
MUX
558R
556
557R
RU/CU
COEF
561
562R
PRE
566
568R
SHAPING
FILTER
COEF
576
572
574
S
D/A
M
399
514
520
516
526
525
SCRMBL
M
530
528
529
SEED
546I
544
542R
542I
549I
548
558I
560I
560R
557I
563
564
562I
570
568I
PRECODE
EQUAL
FILTER
PILOT CHANNEL
DATA AND OTHER
COMMAND & CONTROL
CHANNEL DATA
540
ACC
550
SEED
RNG
510
CONSTANT
13 BIT
BARKER
CODE
~~512~~
P ~~DATA RU/CU~~
405
CPU
1082
CONTROL
LOGIC
TO/FROM
CIRCUITS NEEDING
CONTROL/DATA
TRANSMISSION
MEDIA
24
UP/DOWN
CONVERTER
577

CU ~~28B~~ TRANSMITTER

FIG. ~~28A~~ 32

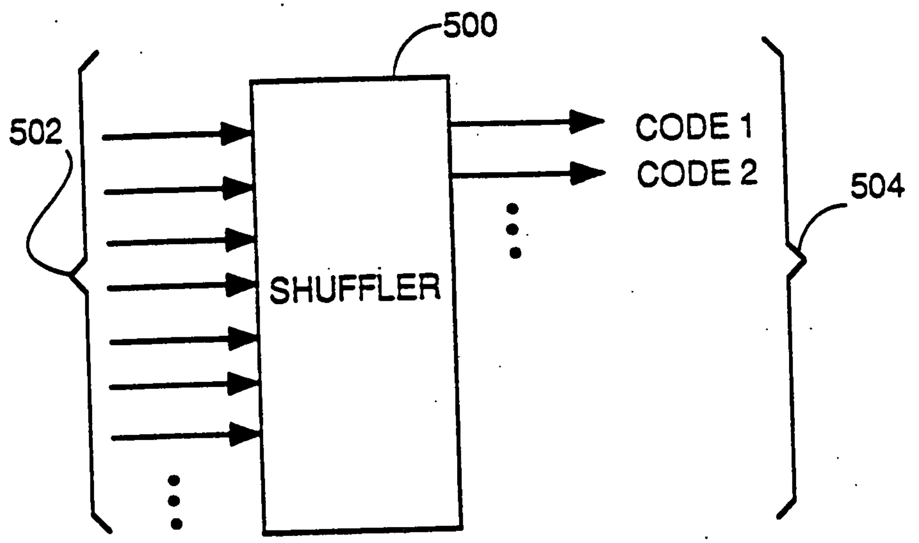
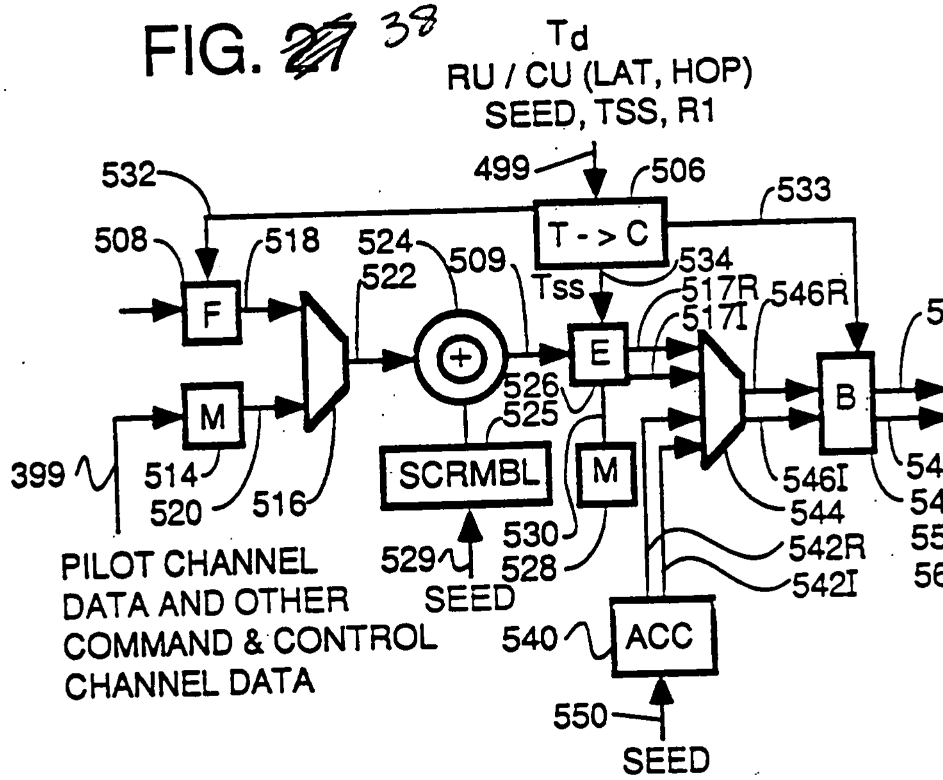
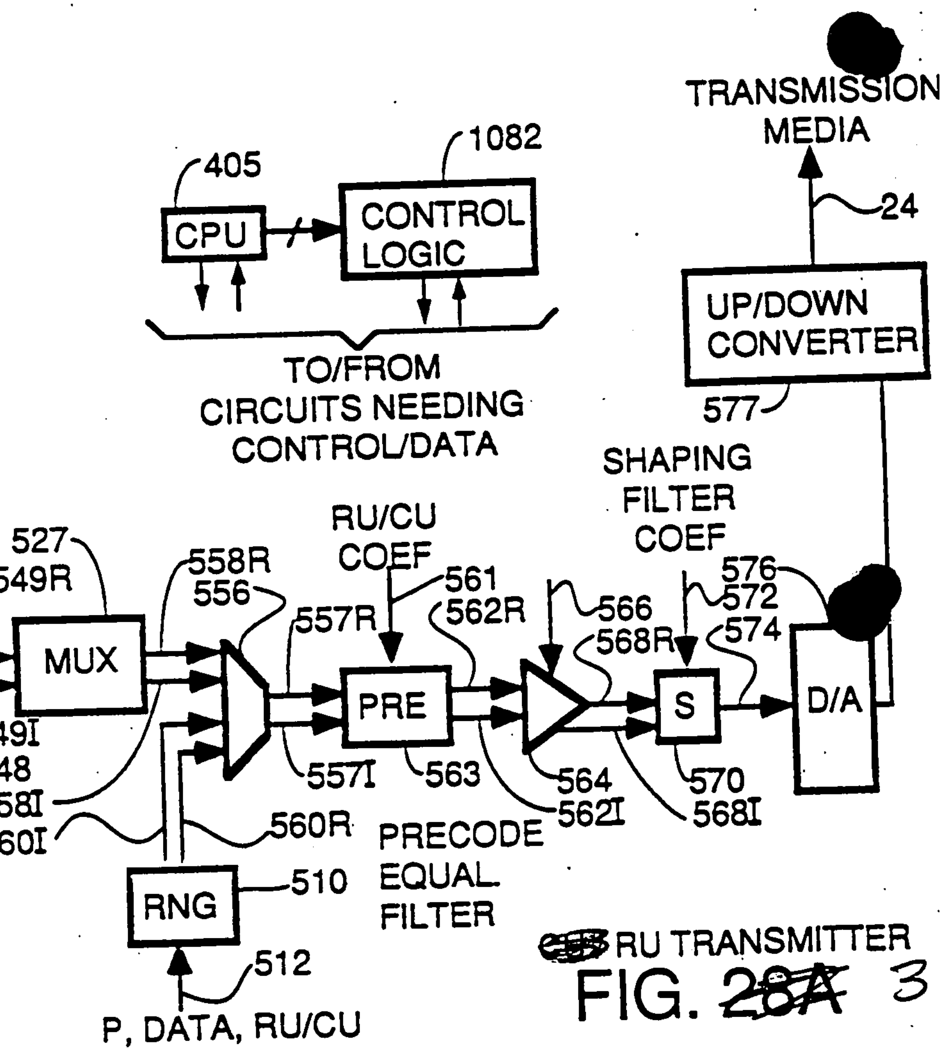

500
502
SHUFFLER
CODE 1
CODE 2
504

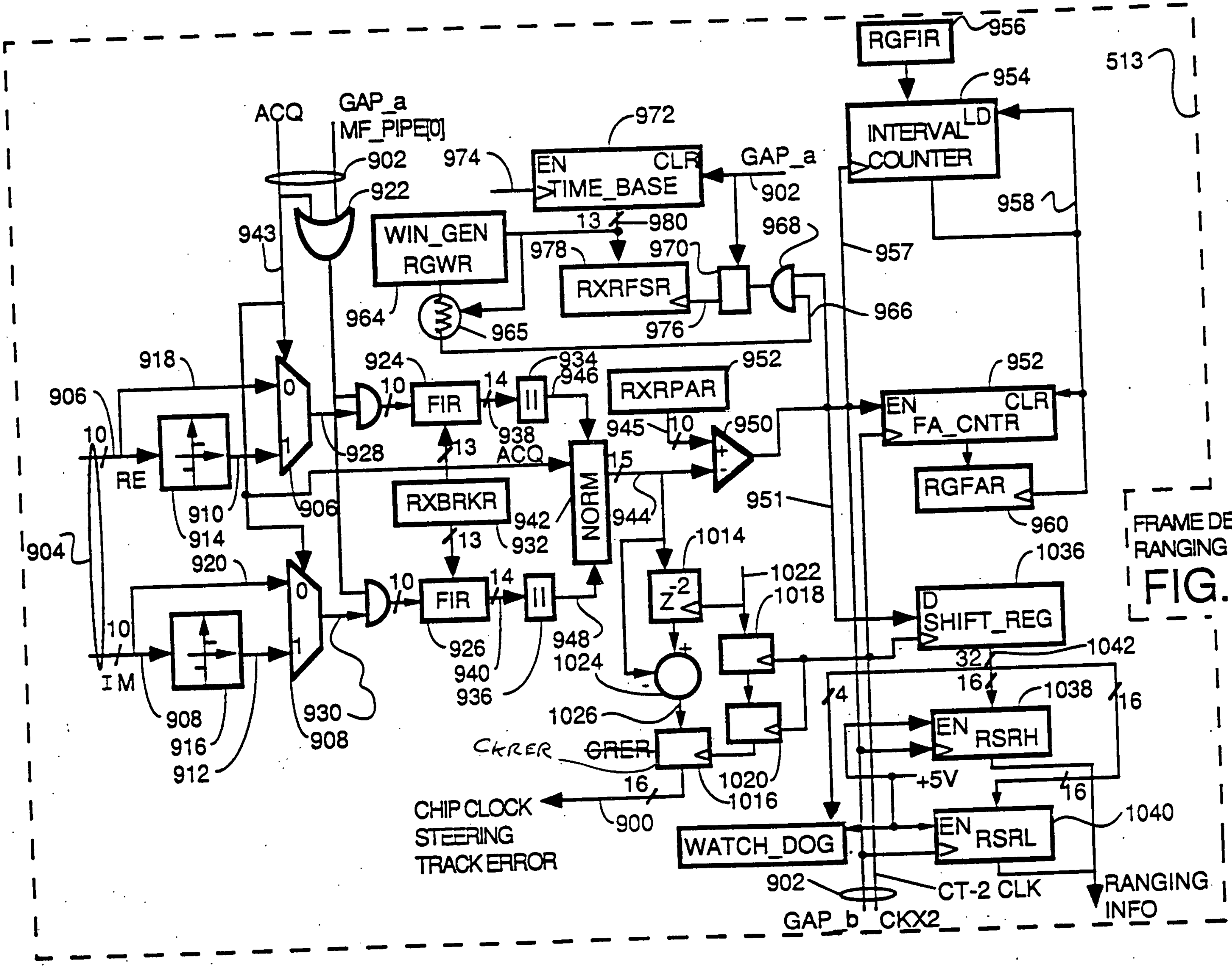
FIG. ~~27~~ 38


Td
RU / CU (LAT, HOP)
SEED, TSS, R1
499
506
T - > C
533
532
508
F
518
524
522
509
534
Tss
E
517R
517I
546R
526
525
M
514
520
516
399
SCRMBL
M
530
528
529
SEED
544
546I
542R
542I
B
ACC
540
550
SEED
PILOT CHANNEL
DATA AND OTHER
COMMAND & CONTROL
CHANNEL DATA


TRANSMISSION
MEDIA
24
UP/DOWN
CONVERTER
577
405
CPU
CONTROL
LOGIC
1082
TO/FROM
CIRCUITS NEEDING
CONTROL/DATA
527
549R
MUX
549I
548
558I
560I
558R
556
557R
RU/CU
COEF
561
562R
PRE
557I
563
560R
RNG
510
512
P, DATA, RU/CU
PRECODE
EQUAL
FILTER
566
568R
564
562I
SHAPING
FILTER
COEF
576
572
574
S
570
568I
D/A

~~28~~ RU TRANSMITTER

FIG. ~~28A~~ 3


RGFIR
956
954
513
INTERVAL
COUNTER
LD
958
ACQ
GAP_a
MF_PIPE[0]
902
922
943
974
EN
CLR
TIME_BASE
972
GAP_a
902
13
980
WIN_GEN
RGWR
978
970
968
RXRFSR
957
964
965
976
966
918
924
10
FIR
14
934
946
RXRPAR
952
952
EN
CLR
FA_CNTR
906
0
1
10
938
13
ACQ
945
10
950
928
RE
15
+
-
RGFAR
910
914
906
RXBRKR
942
932
NORM
944
951
960
904
920
13
1014
1036
0
10
14
z^{-2}
1022
1018
D
SHIFT_REG
10
FIR
948
1024
1042
+
32
I M
1
-
16
1038
16
908
916
912
930
908
926
940
936
4
1026
EN
RSRH
CkRER
~~GRER~~
1020
1016
+5V
16
16
900
1040
CHIP CLOCK
STEERING
TRACK ERROR
WATCH_DOG
EN
RSRL
902
CT-2 CLK
RANGING
INFO
GAP_b
CKX2

FRAME DETECTOR/
RANGING DETECTOR

FIG. ~~38~~ 3

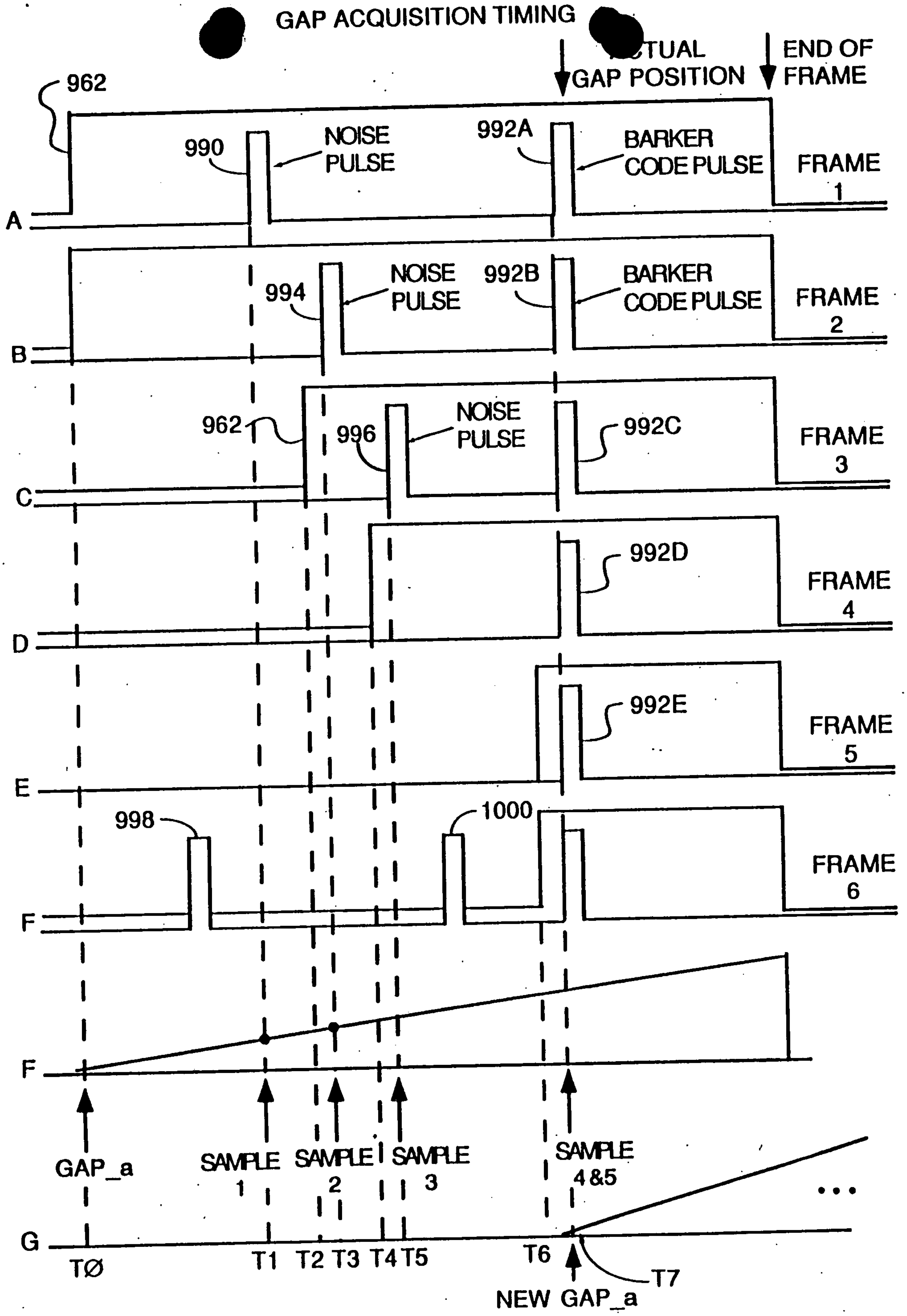

GAP ACQUISITION TIMING
CTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4&5
...
G
TØ
T1
T2
T3
T4
T5
T6
T7
NEW GAP_a

FIG. ~~39~~ 35

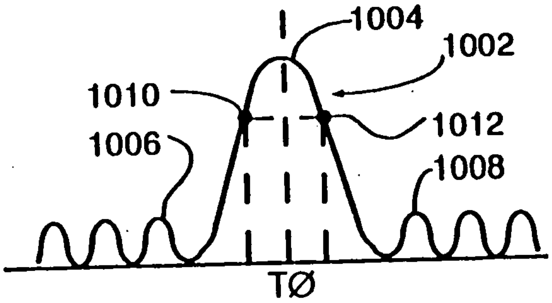

1004
1002
1010
1012
1006
1008
TØ

FIG. ~~40~~ 36

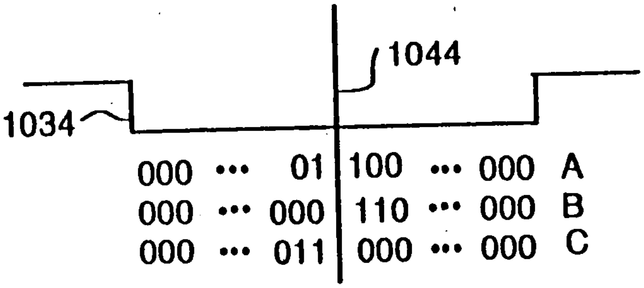

1044
1034
000 ••• 01 | 100 ••• 000 A
000 ••• 000 | 110 ••• 000 B
000 ••• 011 | 000 ••• 000 C

FIG. ~~41~~ 37

FINE TUNING
TO CENTER
BARKER CODE

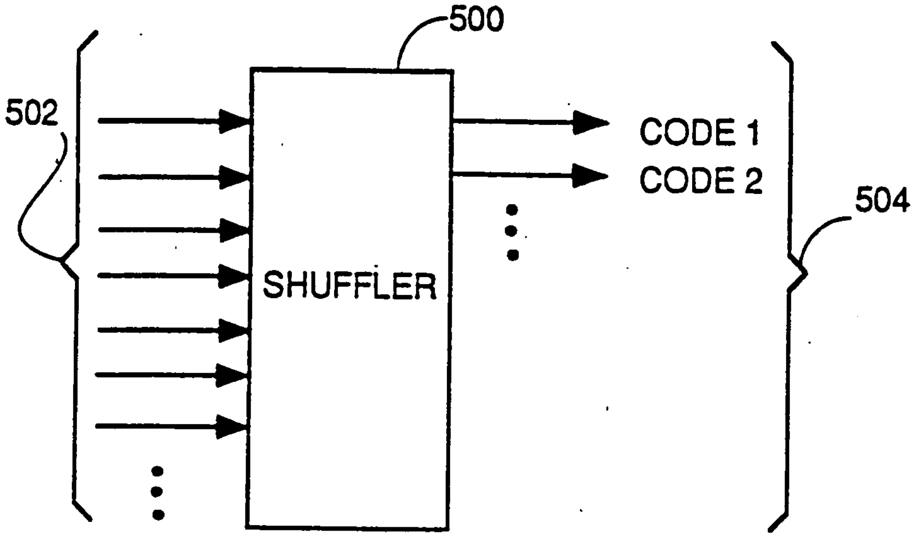

500
502
SHUFFLER
CODE 1
CODE 2
504

FIG. ~~27~~ 38

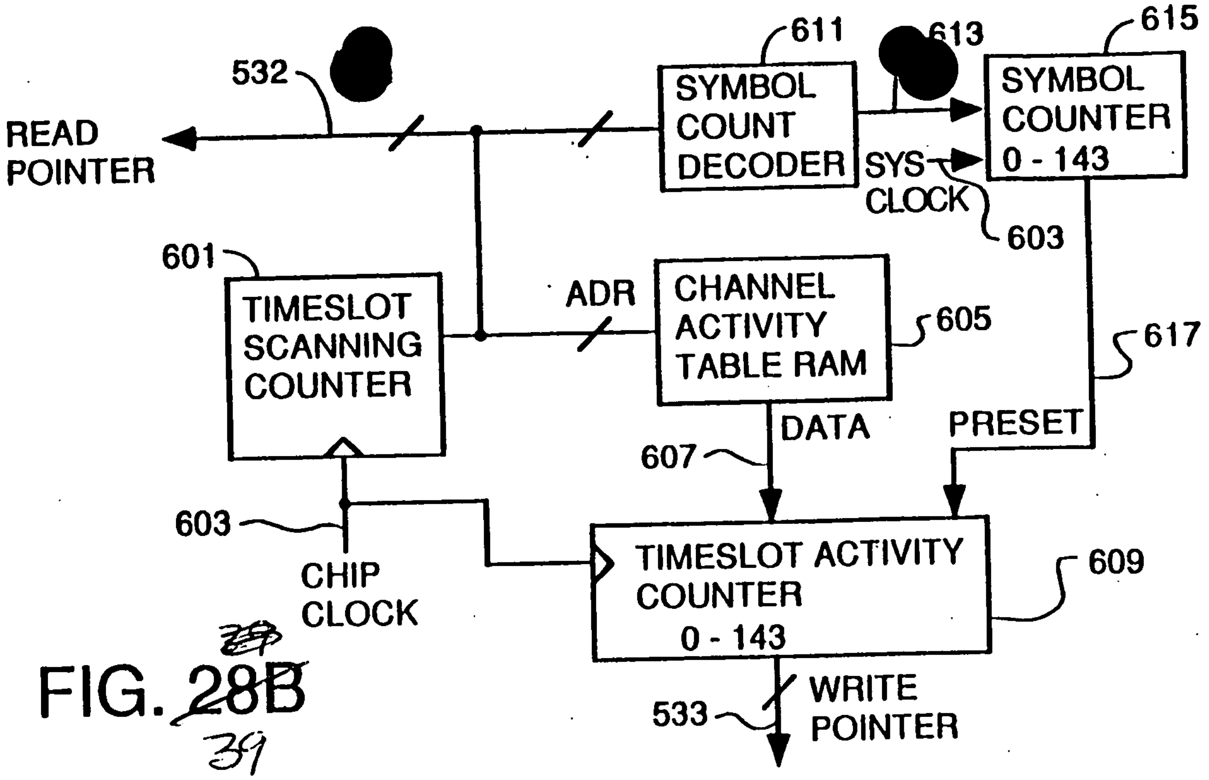

532
READ POINTER
611
SYMBOL COUNT DECODER
613
615
SYMBOL COUNTER 0 - 143
SYS CLOCK
603
601
TIMESLOT SCANNING COUNTER
ADR
CHANNEL ACTIVITY TABLE RAM
605
617
DATA
PRESET
607
603
CHIP CLOCK
TIMESLOT ACTIVITY COUNTER 0 - 143
609
533
WRITE POINTER

FIG. ~~28B~~
~~29~~ 39

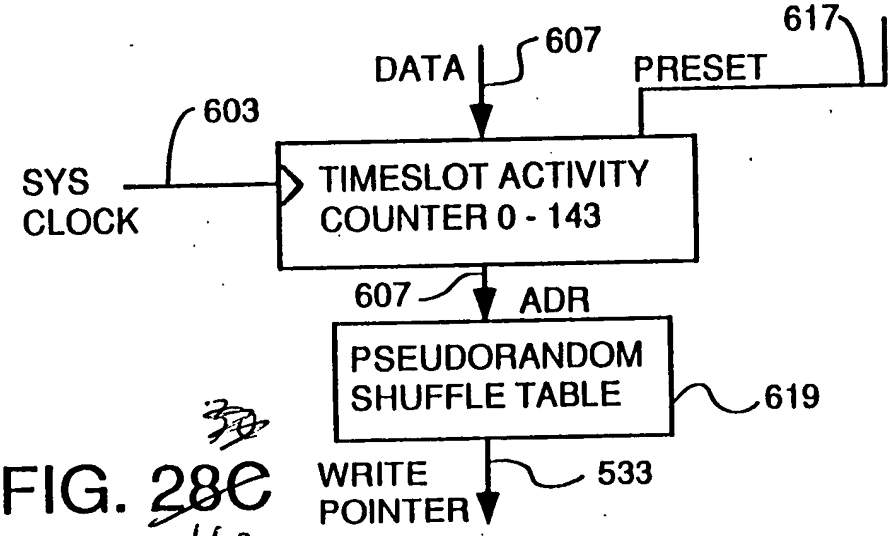

607
DATA
617
PRESET
603
SYS CLOCK
TIMESLOT ACTIVITY COUNTER 0 - 143
607
ADR
PSEUDORANDOM SHUFFLE TABLE
619
WRITE POINTER
533

FIG. ~~28C~~
~~30~~ 40

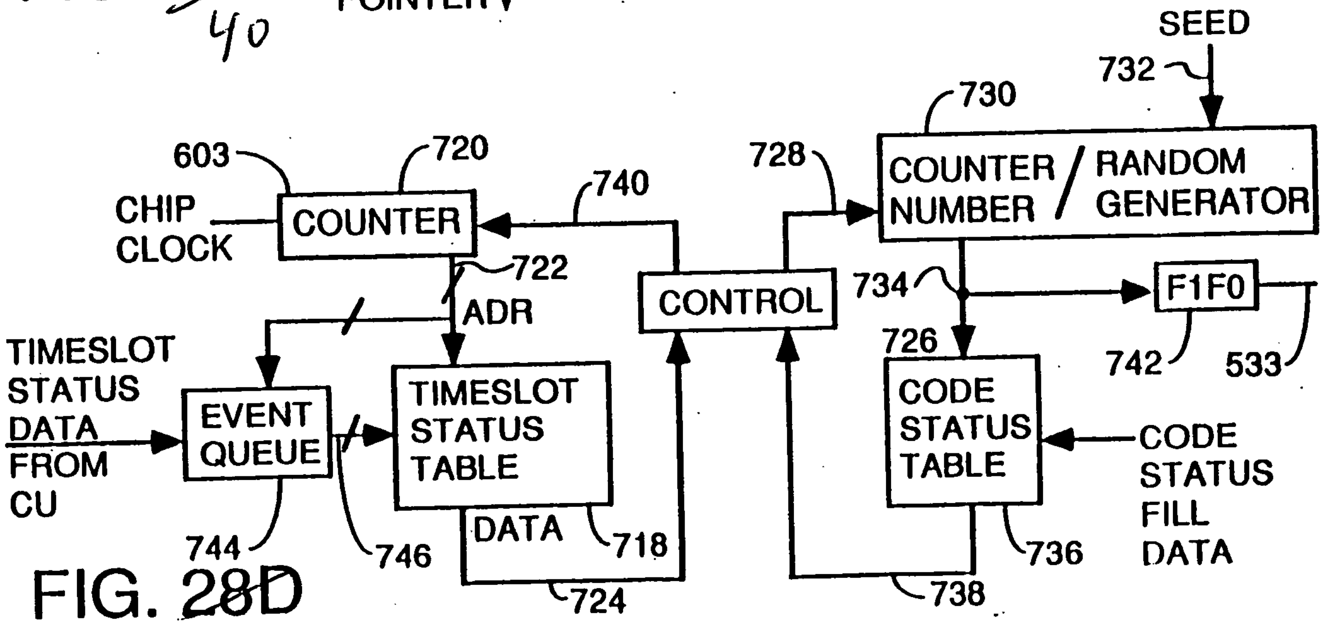

SEED
732
730
COUNTER NUMBER / RANDOM GENERATOR
728
603
720
740
CHIP CLOCK
COUNTER
722
ADR
CONTROL
734
F1F0
726
742
533
TIMESLOT STATUS DATA FROM CU
EVENT QUEUE
TIMESLOT STATUS TABLE
CODE STATUS TABLE
CODE STATUS FILL DATA
DATA
718
744
746
736
724
738

FIG. ~~28D~~
~~33~~ 41

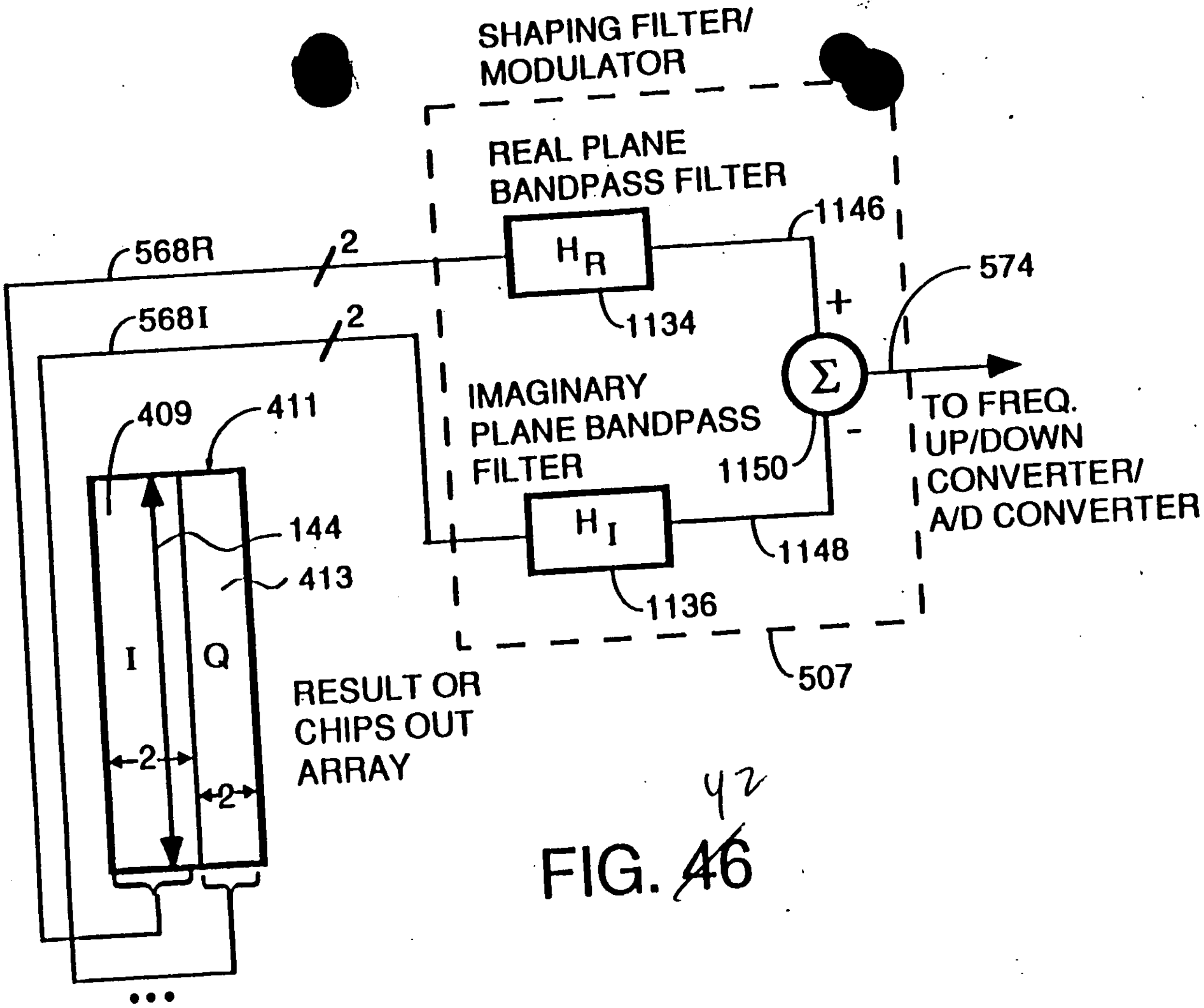

SHAPING FILTER/
MODULATOR
REAL PLANE
BANDPASS FILTER
1146
568R
2
HR
574
568I
2
1134
+
Σ
409
411
IMAGINARY
PLANE BANDPASS
FILTER
TO FREQ.
UP/DOWN
CONVERTER/
A/D CONVERTER
-
1150
HI
144
1148
413
1136
I
Q
507
RESULT OR
CHIPS OUT
ARRAY
2
2
...

FIG. ~~46~~ 42

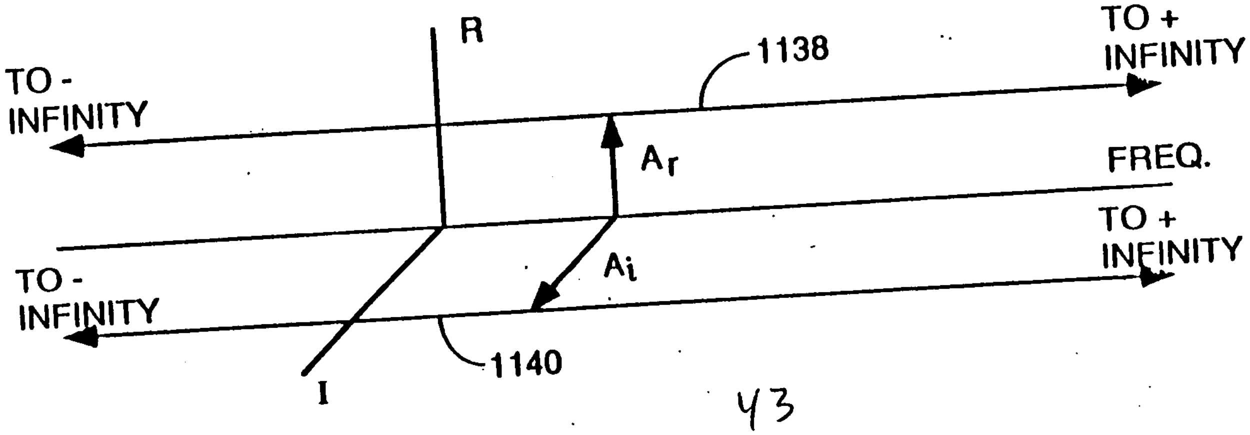

R
1138
TO +
INFINITY
TO -
INFINITY
Ar
FREQ.
TO +
INFINITY
Ai
TO -
INFINITY
1140
I

FIG. ~~47~~ 43

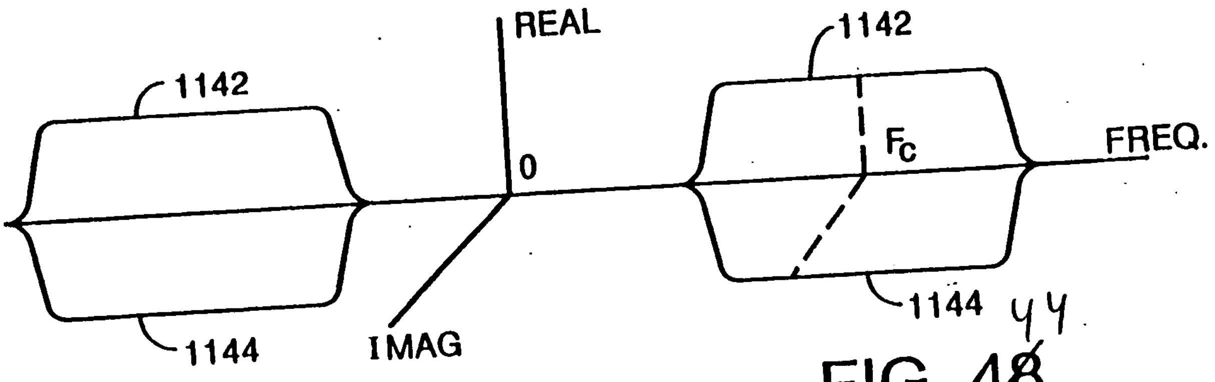
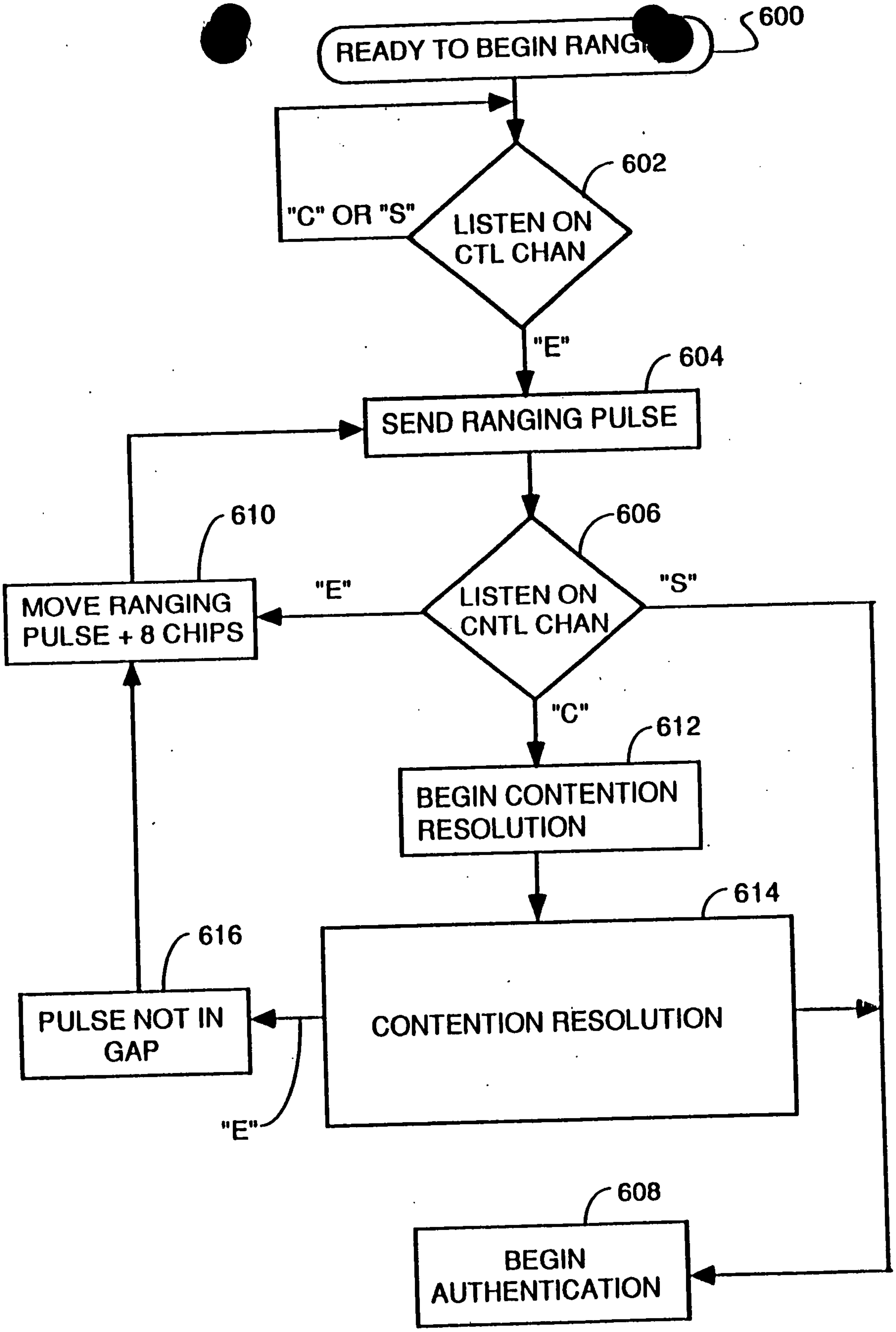
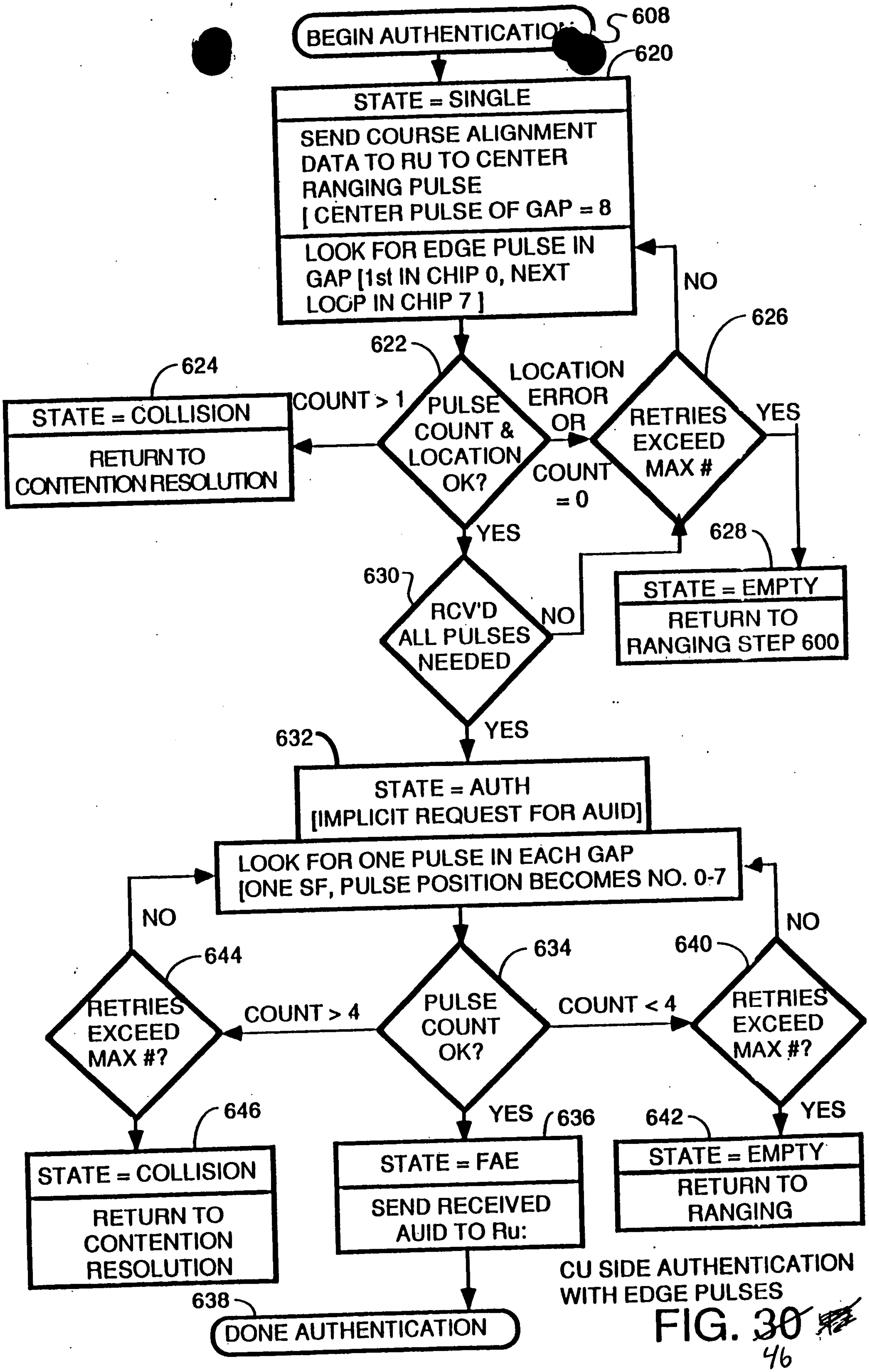

REAL
1142
1142
Fc
FREQ.
0
1144
1144
IMAG

FIG. ~~48~~ 44


READY TO BEGIN RANGING
600
"C" OR "S"
LISTEN ON CTL CHAN
602
"E"
SEND RANGING PULSE
604
610
MOVE RANGING PULSE + 8 CHIPS
"E"
LISTEN ON CNTL CHAN
606
"S"
"C"
612
BEGIN CONTENTION RESOLUTION
614
616
CONTENTION RESOLUTION
PULSE NOT IN GAP
"E"
608
BEGIN AUTHENTICATION

RU RANGING

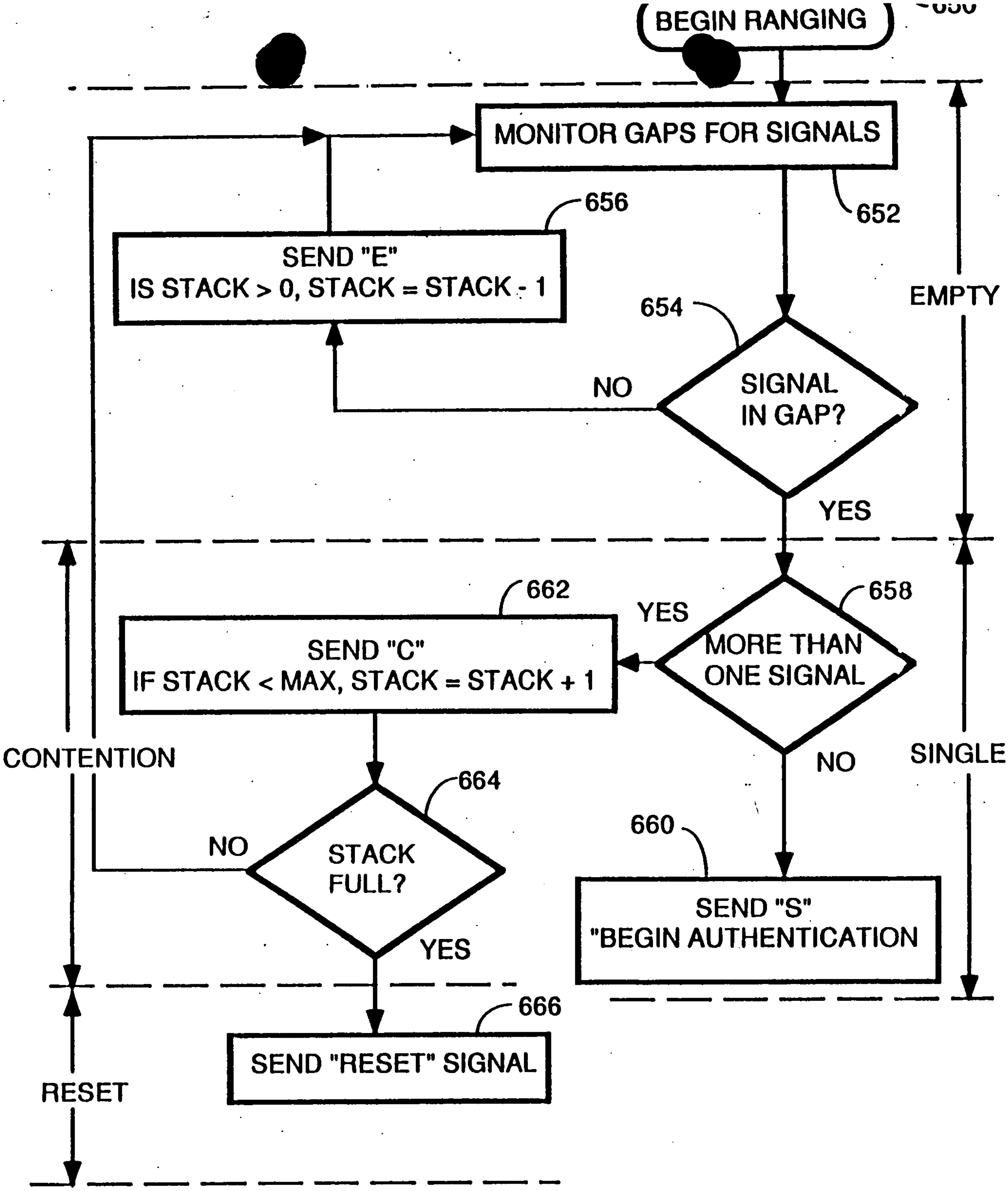
FIG. 29


BEGIN AUTHENTICATION
608
620
STATE = SINGLE
SEND COURSE ALIGNMENT DATA TO RU TO CENTER RANGING PULSE [CENTER PULSE OF GAP = 8
LOOK FOR EDGE PULSE IN GAP [1st IN CHIP 0, NEXT LOOP IN CHIP 7]
NO
626
622
624
STATE = COLLISION
RETURN TO CONTENTION RESOLUTION
COUNT > 1
PULSE COUNT & LOCATION OK?
LOCATION ERROR OR COUNT = 0
RETRIES EXCEED MAX #
YES
YES
628
630
RCV'D ALL PULSES NEEDED
NO
STATE = EMPTY
RETURN TO RANGING STEP 600
YES
632
STATE = AUTH [IMPLICIT REQUEST FOR AUID]
LOOK FOR ONE PULSE IN EACH GAP [ONE SF, PULSE POSITION BECOMES NO. 0-7
NO
NO
644
634
640
RETRIES EXCEED MAX #?
COUNT > 4
PULSE COUNT OK?
COUNT < 4
RETRIES EXCEED MAX #?
646
YES
636
642
YES
STATE = COLLISION
RETURN TO CONTENTION RESOLUTION
STATE = FAE
SEND RECEIVED AUID TO Ru:
STATE = EMPTY
RETURN TO RANGING
638
DONE AUTHENTICATION

CU SIDE AUTHENTICATION WITH EDGE PULSES

FIG. 30

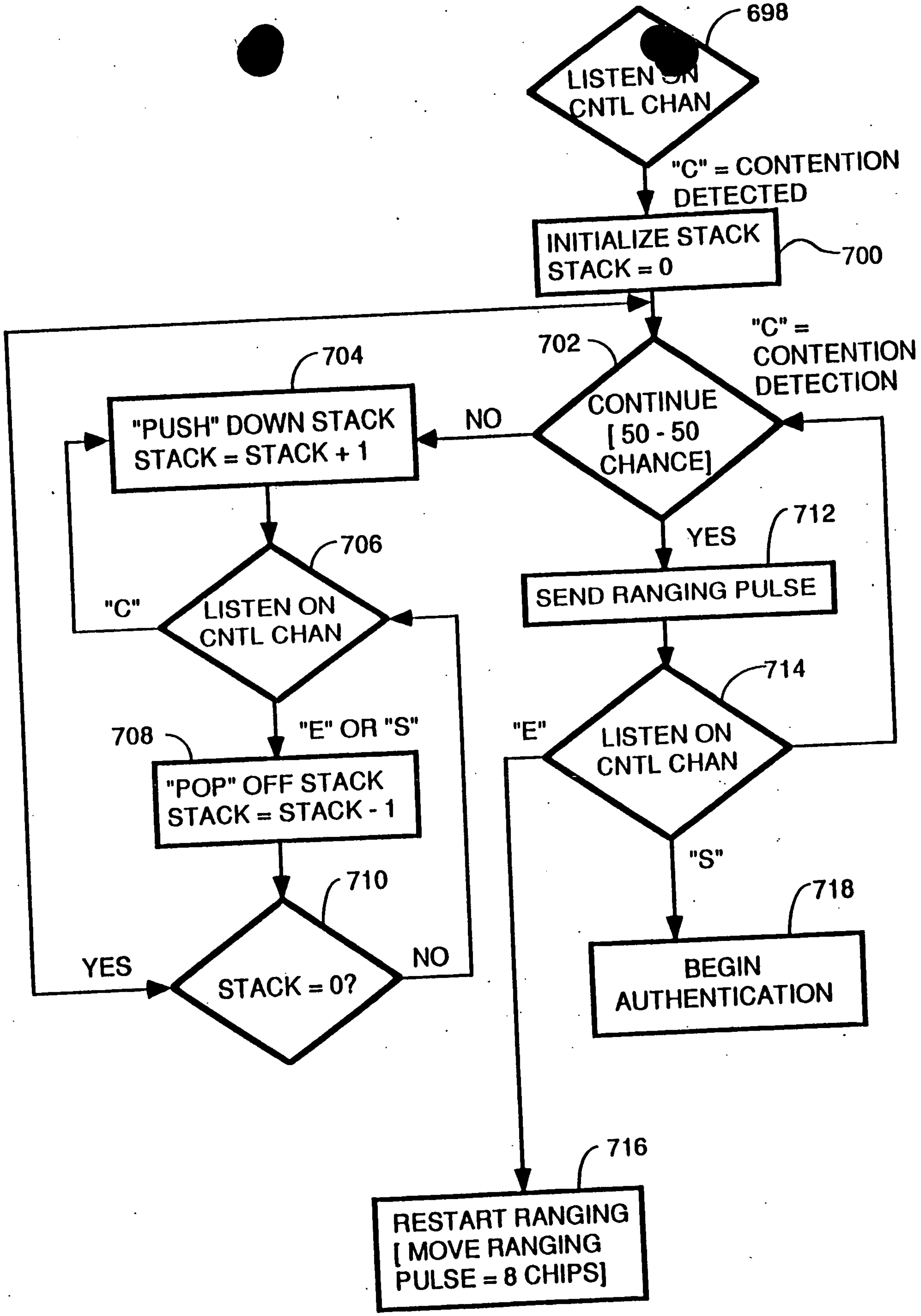
46


BEGIN RANGING
650
MONITOR GAPS FOR SIGNALS
652
656
SEND "E"
IS STACK > 0, STACK = STACK - 1
654
EMPTY
NO
SIGNAL IN GAP?
YES
662
658
YES
SEND "C"
IF STACK < MAX, STACK = STACK + 1
MORE THAN ONE SIGNAL
CONTENTION
664
NO
SINGLE
660
NO
STACK FULL?
SEND "S"
"BEGIN AUTHENTICATION
YES
666
SEND "RESET" SIGNAL
RESET

CU RANGING & CONTENTION RESOLUTION

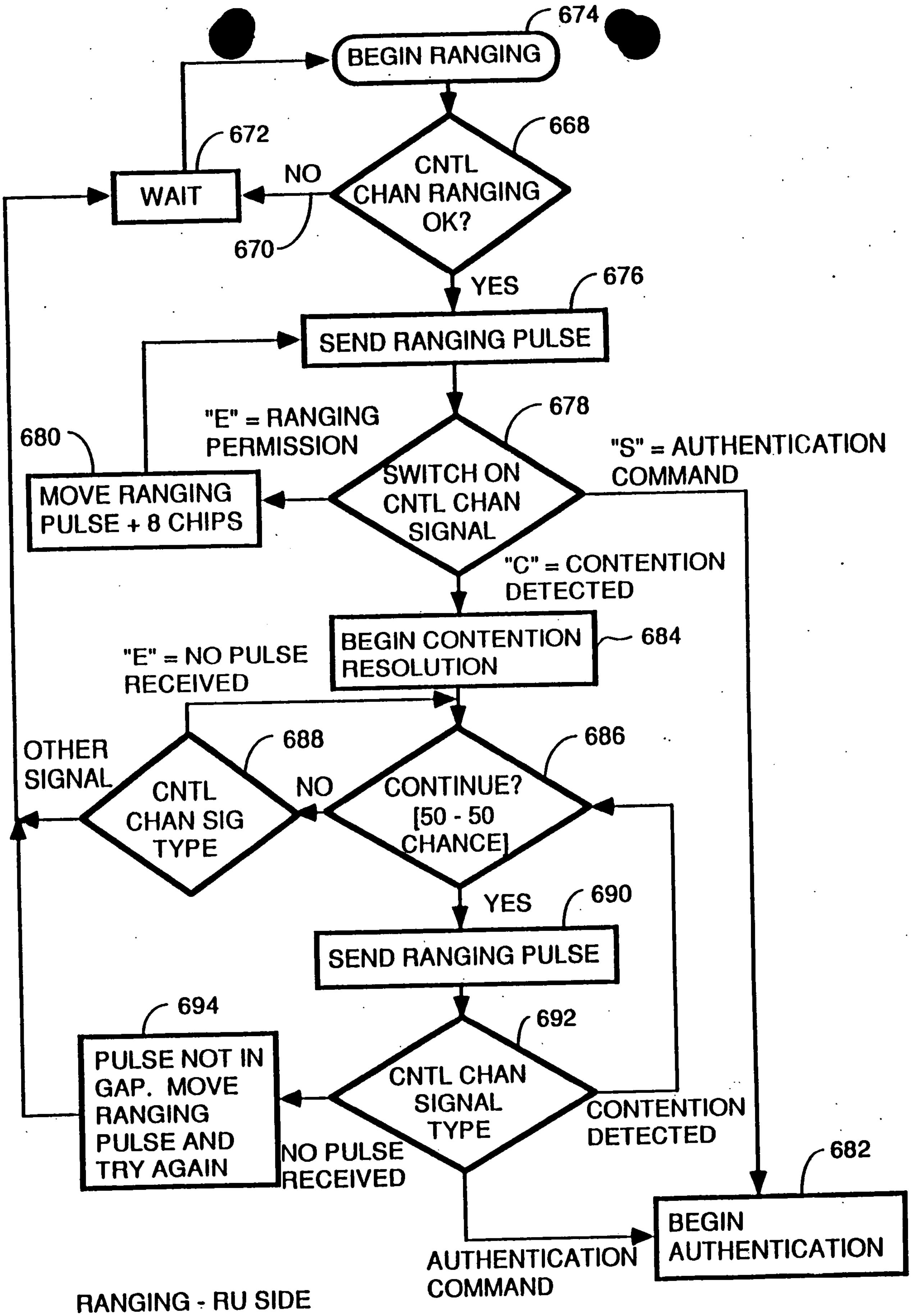
~~RANGING AND CONTENTION RESOLUTION~~
~~CU SIDE~~

FIG. 3~~1~~ ~~48~~
47


698
LISTEN ON CNTL CHAN
"C" = CONTENTION DETECTED
INITIALIZE STACK STACK = 0
700
702
"C" = CONTENTION DETECTION
CONTINUE [50 - 50 CHANCE]
NO
704
"PUSH" DOWN STACK STACK = STACK + 1
YES
712
SEND RANGING PULSE
706
"C"
LISTEN ON CNTL CHAN
"E" OR "S"
708
"POP" OFF STACK STACK = STACK - 1
714
"E"
LISTEN ON CNTL CHAN
"S"
710
718
YES
STACK = 0?
NO
BEGIN AUTHENTICATION
716
RESTART RANGING [MOVE RANGING PULSE = 8 CHIPS]

CONTENTION RESOLUTION - RU
USING BINARY STACK

FIG. ~~33~~ ~~49~~


674
BEGIN RANGING
668
CNTL CHAN RANGING OK?
NO
670
672
WAIT
YES
676
SEND RANGING PULSE
678
SWITCH ON CNTL CHAN SIGNAL
"E" = RANGING PERMISSION
680
MOVE RANGING PULSE + 8 CHIPS
"S" = AUTHENTICATION COMMAND
"C" = CONTENTION DETECTED
684
BEGIN CONTENTION RESOLUTION
"E" = NO PULSE RECEIVED
OTHER SIGNAL
688
CNTL CHAN SIG TYPE
NO
686
CONTINUE? [50 - 50 CHANCE]
YES
690
SEND RANGING PULSE
694
PULSE NOT IN GAP. MOVE RANGING PULSE AND TRY AGAIN
692
CNTL CHAN SIGNAL TYPE
NO PULSE RECEIVED
CONTENTION DETECTED
682
BEGIN AUTHENTICATION
AUTHENTICATION COMMAND

RANGING - RU SIDE
BINARY TREE
ALGORITHM

FIG. ~~32~~

~~50~~

49

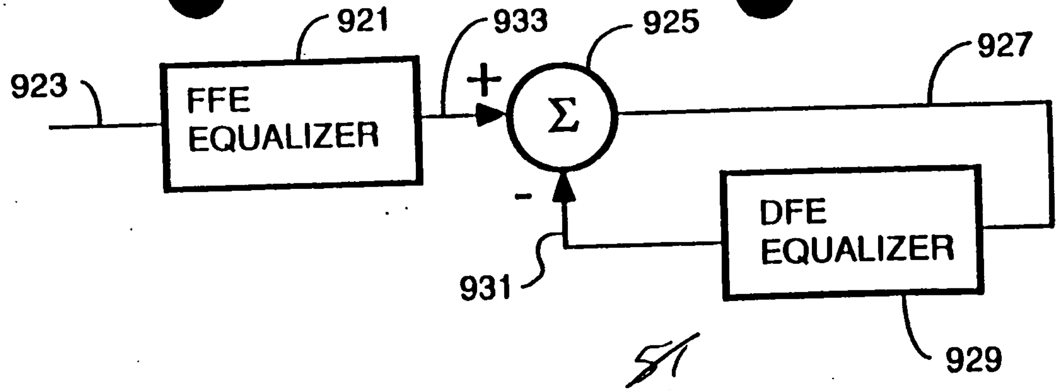
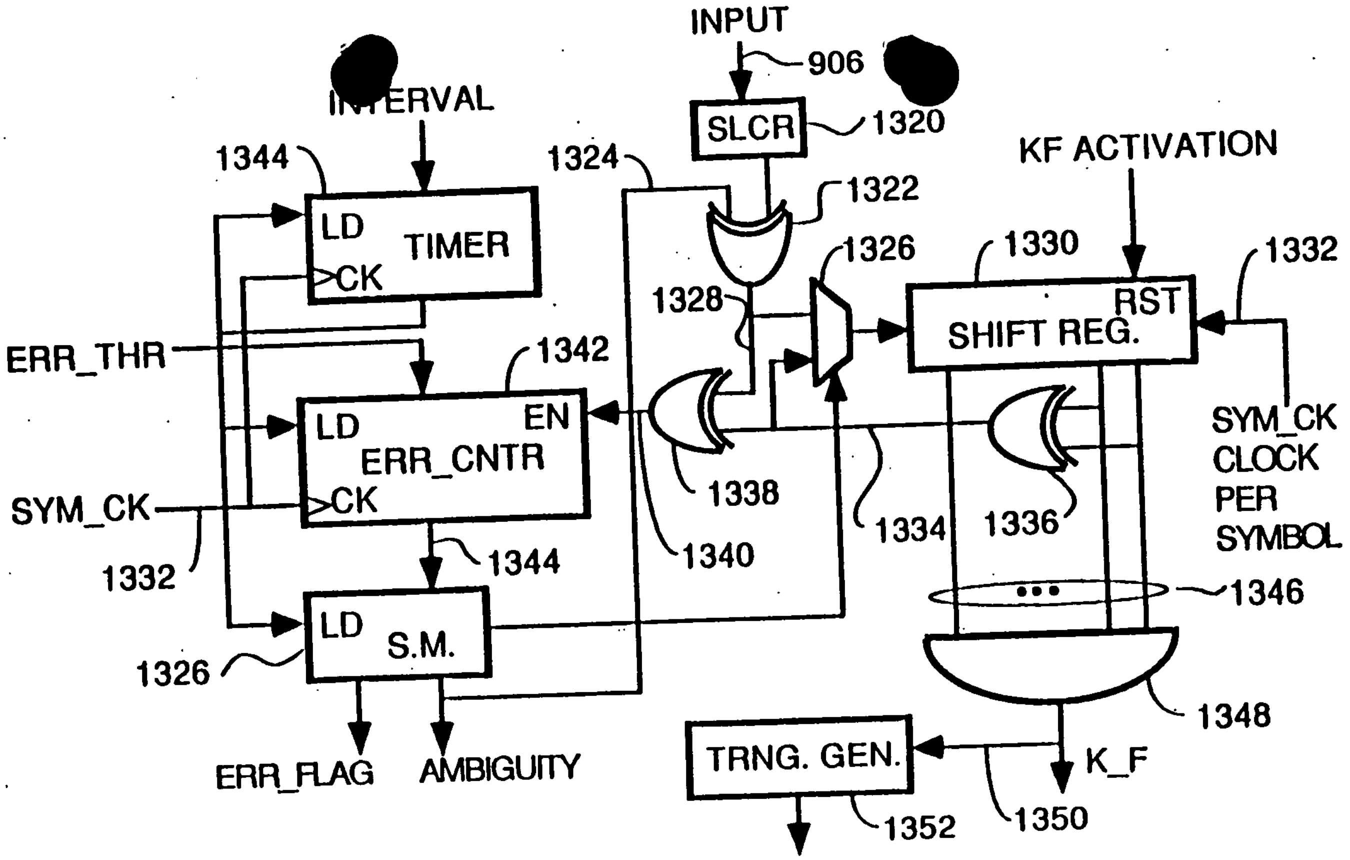
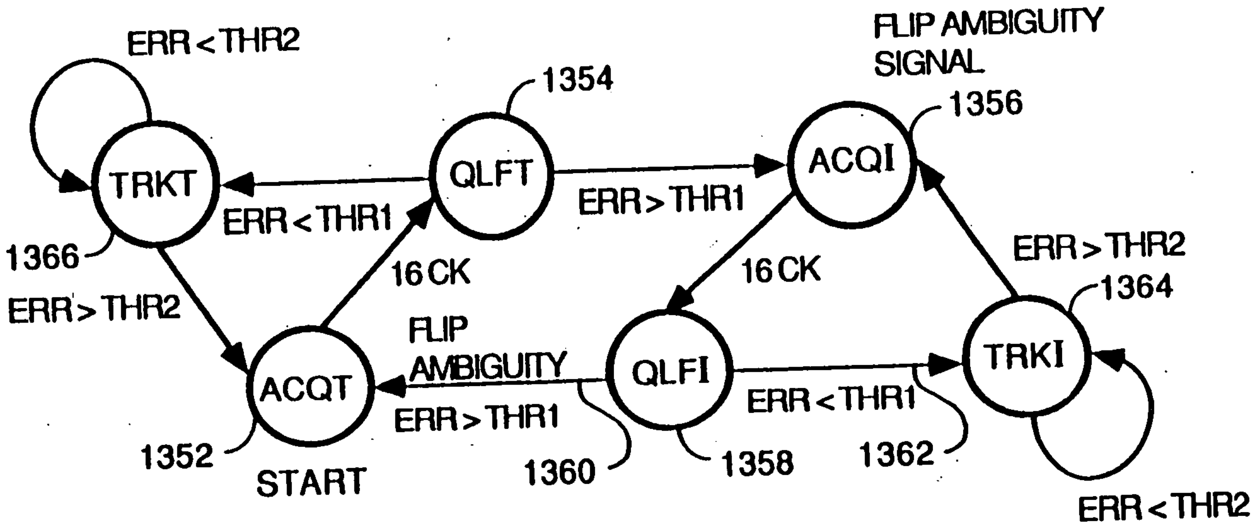

921
933
925
927
923
FFE EQUALIZER
+
Σ
-
DFE EQUALIZER
931
929

FIG. ~~37~~ ~~51~~ 50


INPUT
906
INTERVAL
SLCR
1320
1324
1322
1344
LD
TIMER
CK
KF ACTIVATION
1326
1330
1332
1328
RST
SHIFT REG.
ERR_THR
1342
LD
EN
ERR_CNTR
CK
SYM_CK
1338
1334
1336
SYM_CK CLOCK PER SYMBOL
1332
1344
1340
1346
LD
S.M.
1326
1348
ERR_FLAG
AMBIGUITY
TRNG. GEN.
K_F
1352
1350

FRAME DETECTOR
FRAME SYNC/KILOFRAME DETECT

FIG. ~~52~~
51


ERR < THR2
1354
FLIP AMBIGUITY SIGNAL
1356
TRKT
QLFT
ACQI
ERR < THR1
ERR > THR1
1366
16 CK
16 CK
ERR > THR2
ERR > THR2
1364
FLIP AMBIGUITY
QLFI
TRKI
ACQT
ERR > THR1
ERR < THR1
1352
1360
1358
1362
START
ERR < THR2

STATE MACHINE

FIG. ~~53~~
52

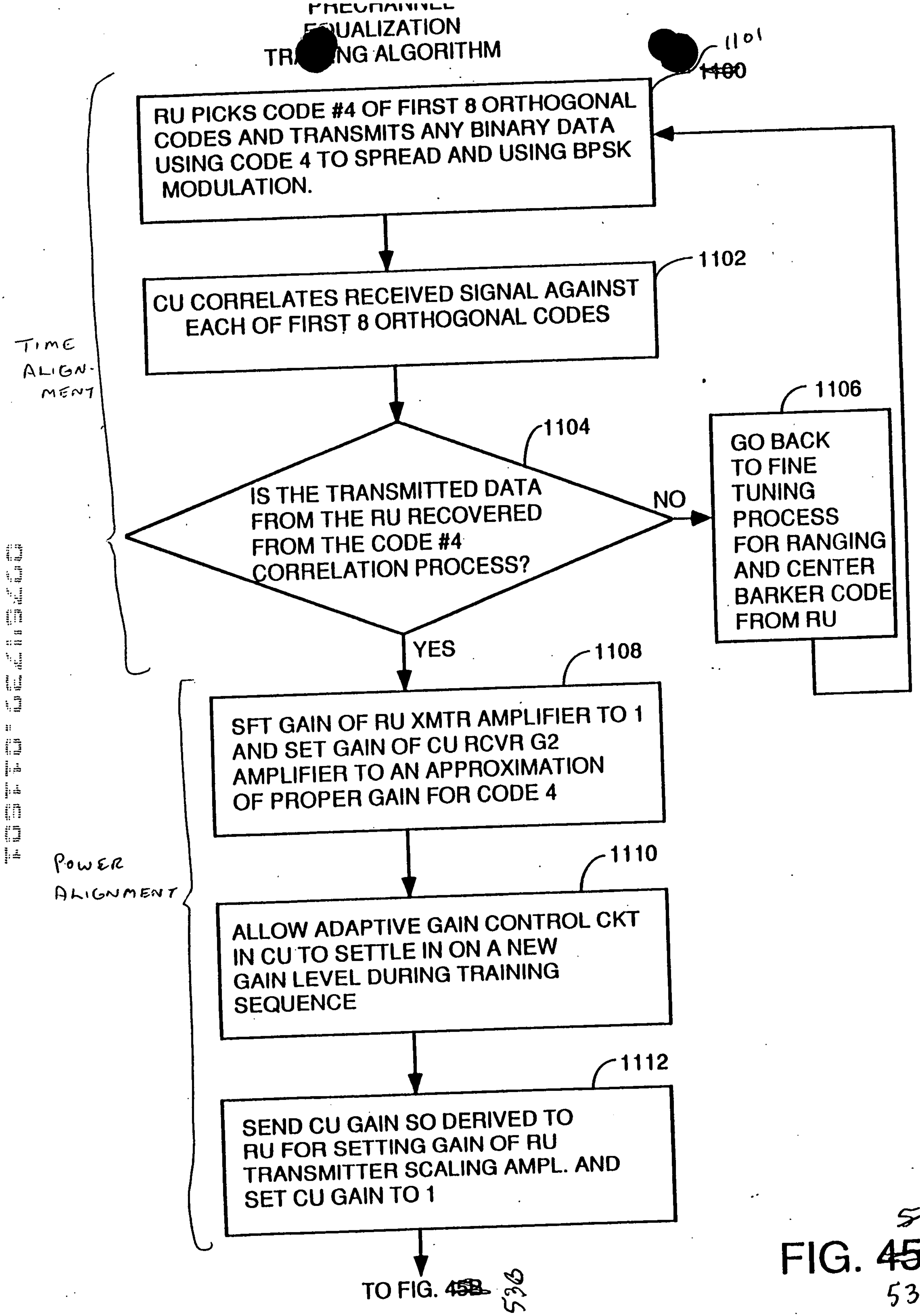
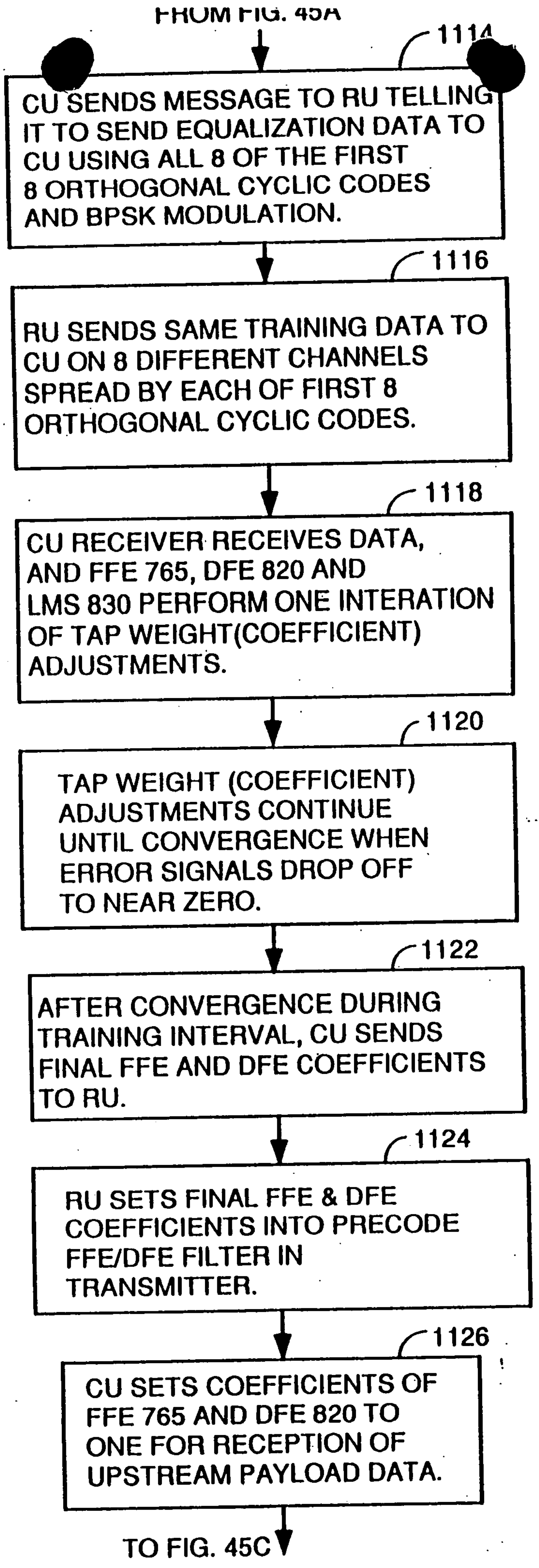

PRECHANNEL
EQUALIZATION
TRA[illegible]NG ALGORITHM
1101
~~1400~~
RU PICKS CODE #4 OF FIRST 8 ORTHOGONAL CODES AND TRANSMITS ANY BINARY DATA USING CODE 4 TO SPREAD AND USING BPSK MODULATION.
1102
CU CORRELATES RECEIVED SIGNAL AGAINST EACH OF FIRST 8 ORTHOGONAL CODES
TIME ALIGNMENT
1104
IS THE TRANSMITTED DATA FROM THE RU RECOVERED FROM THE CODE #4 CORRELATION PROCESS?
NO
1106
GO BACK TO FINE TUNING PROCESS FOR RANGING AND CENTER BARKER CODE FROM RU
YES
1108
SFT GAIN OF RU XMTR AMPLIFIER TO 1 AND SET GAIN OF CU RCVR G2 AMPLIFIER TO AN APPROXIMATION OF PROPER GAIN FOR CODE 4
POWER ALIGNMENT
1110
ALLOW ADAPTIVE GAIN CONTROL CKT IN CU TO SETTLE IN ON A NEW GAIN LEVEL DURING TRAINING SEQUENCE
1112
SEND CU GAIN SO DERIVED TO RU FOR SETTING GAIN OF RU TRANSMITTER SCALING AMPL. AND SET CU GAIN TO 1
TO FIG. ~~45B~~ 53B

FIG. ~~45A~~ ~~54A~~ 53A

UPSTREAM
EQUALIZATION



CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.

RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.

CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.

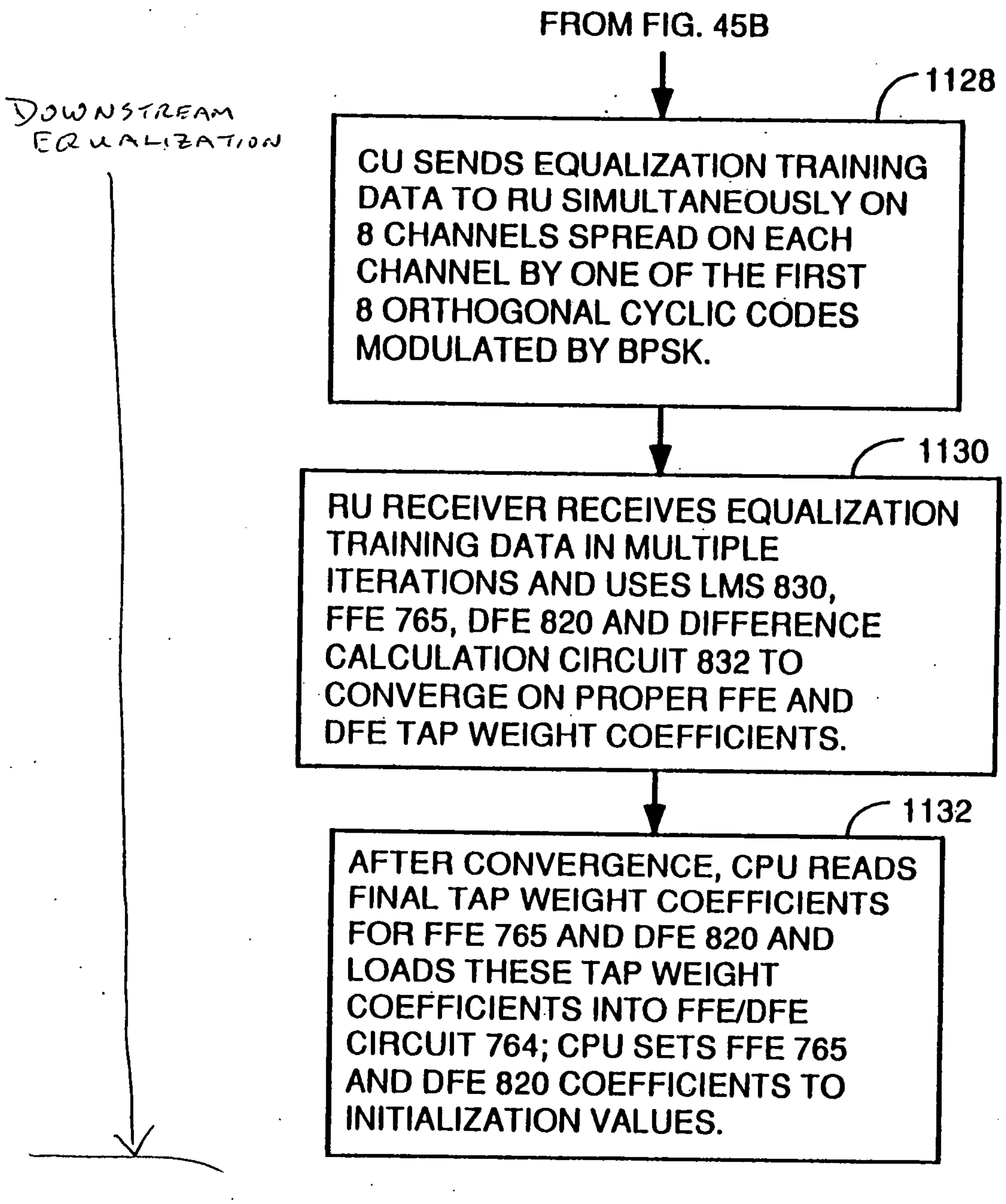
TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.

AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.

RU SETS FINAL FFE & DFE COEFFICIENTS INTO PRECODE FFE/DFE FILTER IN TRANSMITTER.

CU SETS COEFFICIENTS OF FFE 765 AND DFE 820 TO ONE FOR RECEPTION OF UPSTREAM PAYLOAD DATA.

FIG. ~~45B~~ ~~54B~~ 53B



CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.

RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.

AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND LOADS THESE TAP WEIGHT COEFFICIENTS INTO FFE/DFE CIRCUIT 764; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

54C

FIG. ~~45C~~

53C

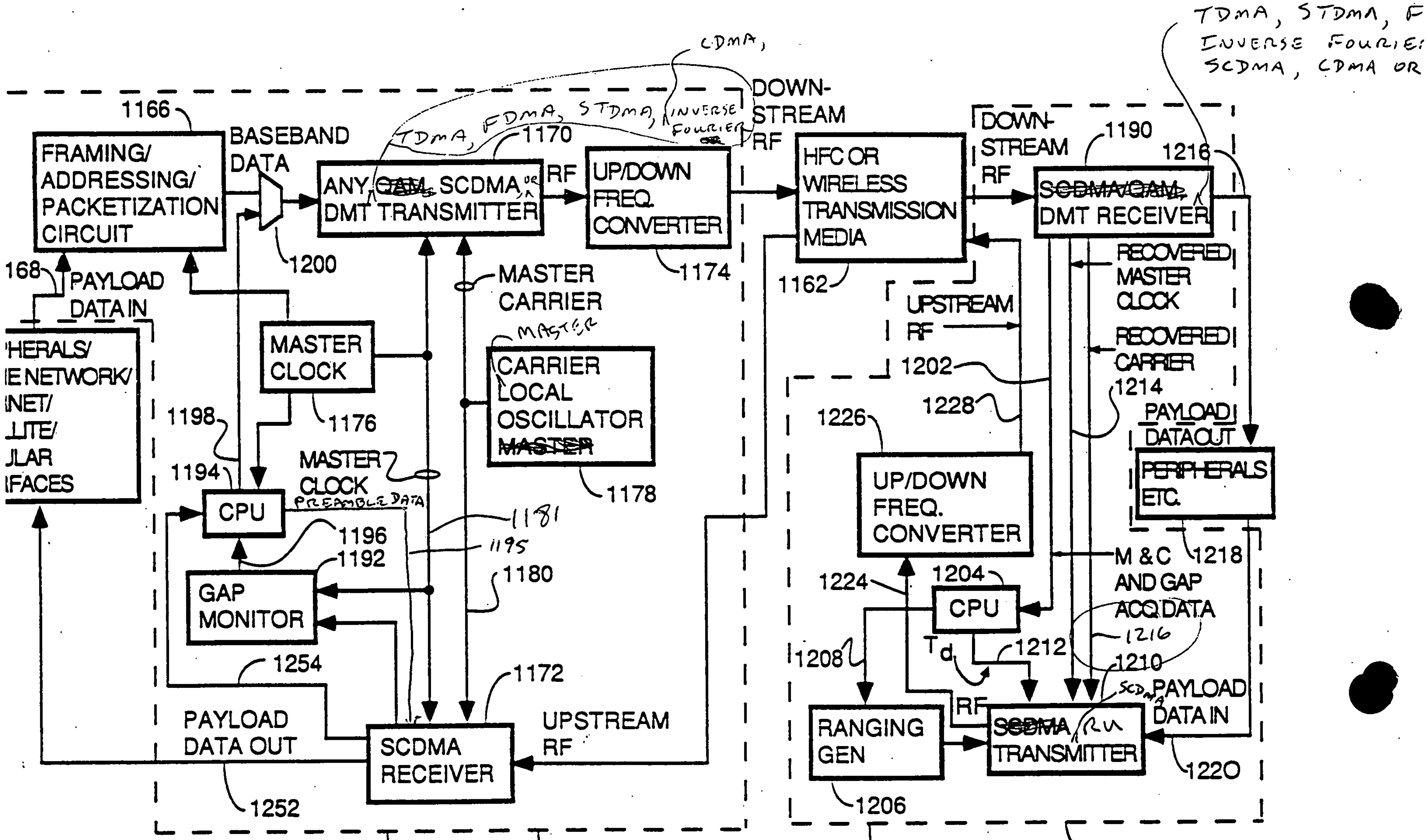
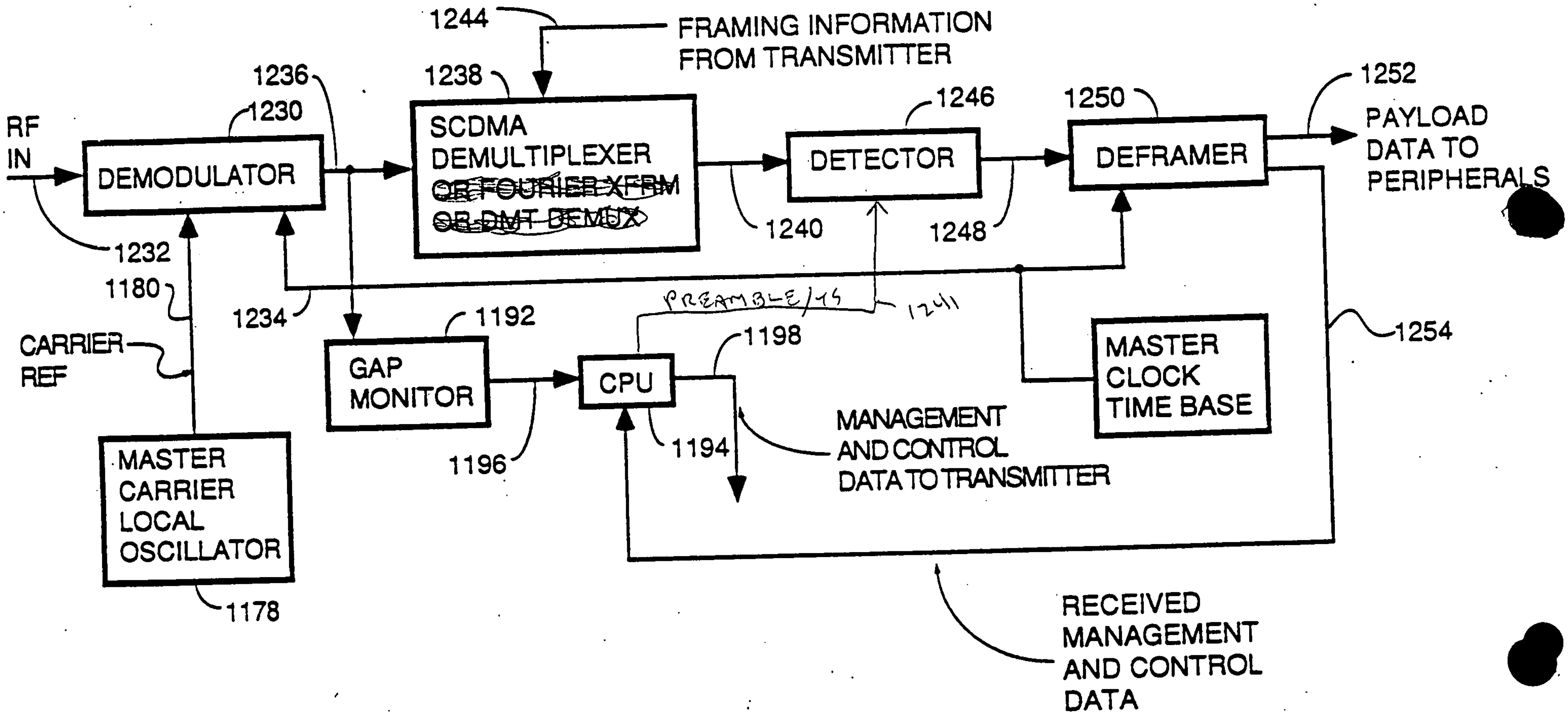
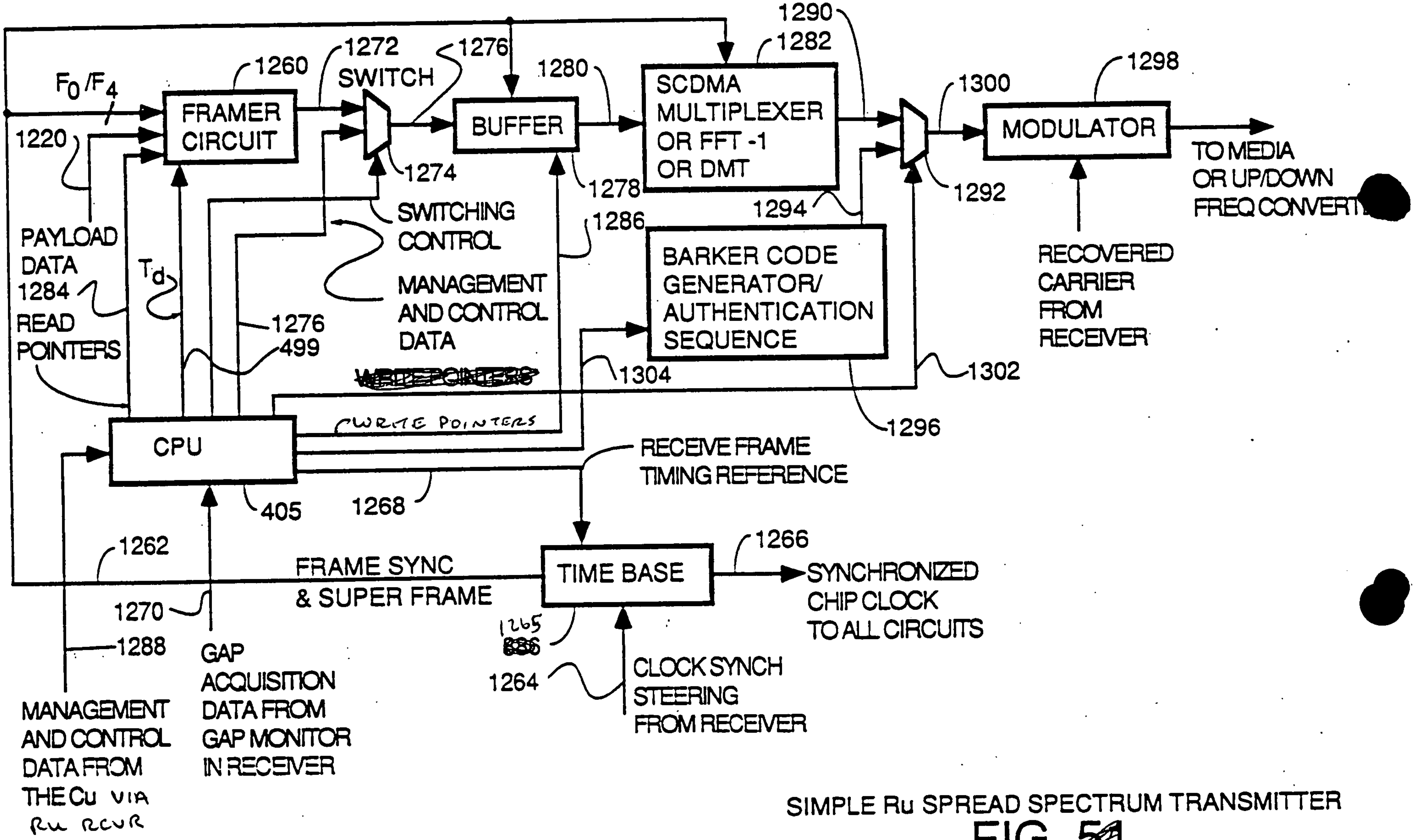
TDMA, STDMA, F
INVERSE FOURIE
SCDMA, CDMA OR
CDMA,
TDMA, FDMA, STDMA, INVERSE FOURIER ~~OR~~
1166
FRAMING/ ADDRESSING/ PACKETIZATION CIRCUIT
BASEBAND DATA
1200
1170
ANY ~~QAM~~ SCDMA OR DMT TRANSMITTER
RF
UP/DOWN FREQ. CONVERTER
1174
DOWN-STREAM RF
HFC OR WIRELESS TRANSMISSION MEDIA
1162
DOWN-STREAM RF
1190
1216
~~SCDMA/QAM~~ DMT RECEIVER
RECOVERED MASTER CLOCK
RECOVERED CARRIER
1214
PAYLOAD DATA OUT
PERIPHERALS ETC.
1218
168
PAYLOAD DATA IN
HERALS/ E NETWORK/ NET/ LITE/ JLAR IFACES
MASTER CLOCK
1176
MASTER CARRIER
MASTER
CARRIER LOCAL OSCILLATOR ~~MASTER~~
1178
1198
1194
CPU
MASTER CLOCK
PREAMBLE DATA
1181
1195
1196
1192
1180
GAP MONITOR
1254
1172
PAYLOAD DATA OUT
SCDMA RECEIVER
UPSTREAM RF
1252
1160
Cu MODEM
UPSTREAM RF
1202
1228
1226
UP/DOWN FREQ. CONVERTER
1224
1204
CPU
M & C AND GAP ACQ DATA
1216
1210
1208
T_d
1212
RF
RANGING GEN
SCDMA
~~SCDMA~~ RU TRANSMITTER
PAYLOAD DATA IN
1220
1206
1164
Ru MODEM

FIG. ~~49~~ ~~55~~ 54


RF IN
DEMODULATOR
1230
1232
1236
1180
CARRIER REF
1234
MASTER CARRIER LOCAL OSCILLATOR
1178
1244
FRAMING INFORMATION FROM TRANSMITTER
1238
SCDMA DEMULTIPLEXER ~~OR FOURIER XFRM OR DMT DEMUX~~
1240
GAP MONITOR
1192
1196
CPU
1194
1198
PREAMBLE/TS
1241
MANAGEMENT AND CONTROL DATA TO TRANSMITTER
1246
DETECTOR
1248
1250
DEFRAMER
MASTER CLOCK TIME BASE
1252
PAYLOAD DATA TO PERIPHERALS
1254
RECEIVED MANAGEMENT AND CONTROL DATA

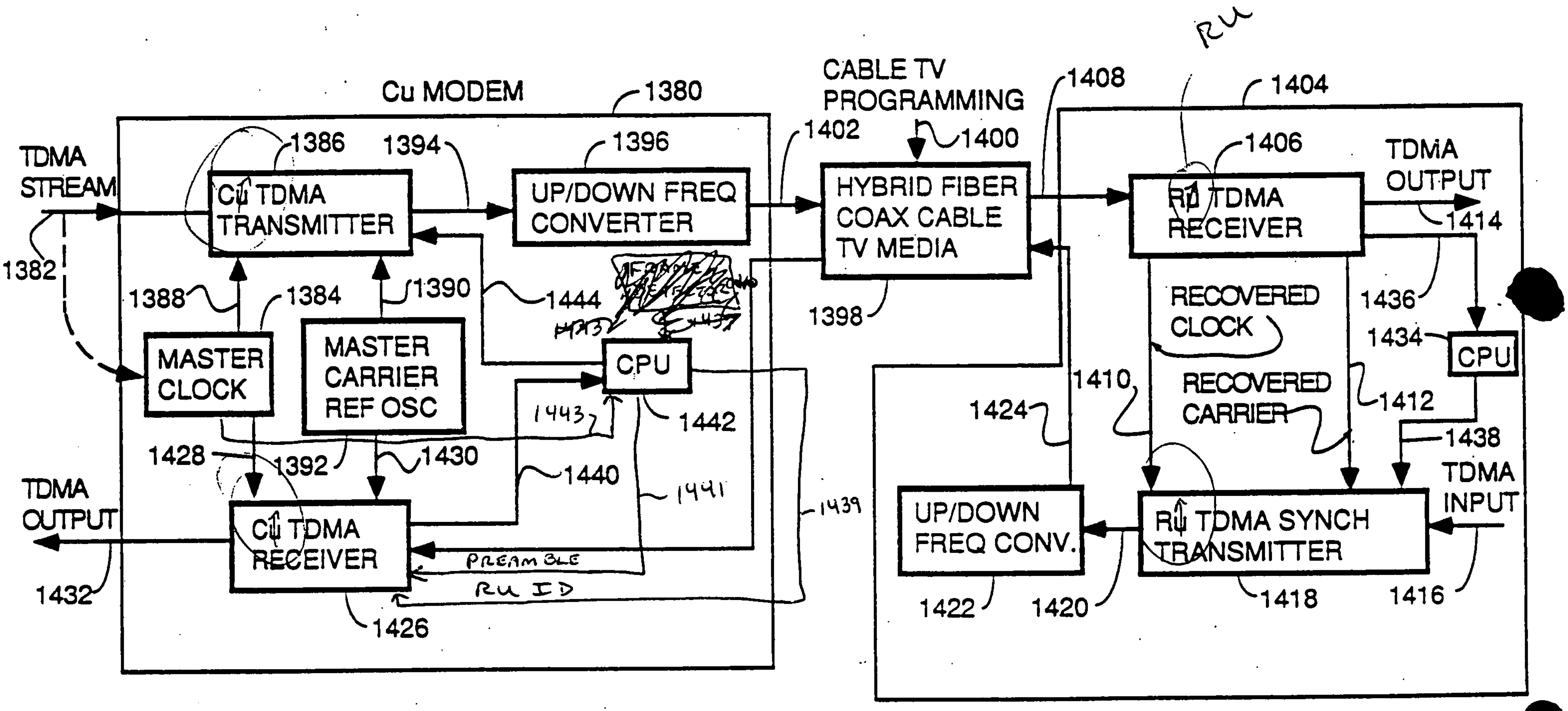
SIMPLE Cu SPREAD SPECTRUM RECEIVER

FIG. ~~50~~ ~~56~~ 55


FRAMER CIRCUIT
1260
F_0/F_4
1220
PAYLOAD DATA
1284
READ POINTERS
T_d
SWITCH
1272
1276
1274
SWITCHING CONTROL
MANAGEMENT AND CONTROL DATA
~~WRITE POINTERS~~
WRITE POINTERS
1276
499
BUFFER
1280
1278
1286
SCDMA MULTIPLEXER OR FFT -1 OR DMT
1290
1282
1294
BARKER CODE GENERATOR/ AUTHENTICATION SEQUENCE
1304
1296
1300
1292
1302
MODULATOR
1298
TO MEDIA OR UP/DOWN FREQ CONVERT
RECOVERED CARRIER FROM RECEIVER
CPU
405
1268
RECEIVE FRAME TIMING REFERENCE
TIME BASE
1266
SYNCHRONIZED CHIP CLOCK TO ALL CIRCUITS
1262
FRAME SYNC & SUPER FRAME
1270
1288
1265
~~886~~
1264
CLOCK SYNCH STEERING FROM RECEIVER
GAP ACQUISITION DATA FROM GAP MONITOR IN RECEIVER
MANAGEMENT AND CONTROL DATA FROM THE Cu VIA Ru RCVR

SIMPLE Ru SPREAD SPECTRUM TRANSMITTER

FIG. ~~51~~ ~~57~~ 56


RU
Cu MODEM
1380
TDMA STREAM
1382
1386
Cu TDMA TRANSMITTER
1394
1396
UP/DOWN FREQ CONVERTER
1388
1384
MASTER CLOCK
MASTER CARRIER REF OSC
1390
1444
1443
1437
CPU
1442
1443
1428
1392
1430
1440
1441
TDMA OUTPUT
Cu TDMA RECEIVER
PREAMBLE
RU ID
1432
1426
1439
CABLE TV PROGRAMMING
1402
1400
HYBRID FIBER COAX CABLE TV MEDIA
1398
1408
1404
1406
RU TDMA RECEIVER
TDMA OUTPUT
1414
RECOVERED CLOCK
1436
1434
CPU
1410
RECOVERED CARRIER
1412
1424
1438
TDMA INPUT
UP/DOWN FREQ CONV.
RU TDMA SYNCH TRANSMITTER
1422
1420
1418
1416

SYNCHRONOUS TDMA SYSTEM

FIG. ~~54~~ ~~58~~ 57

OFFSET	1B ASIC		2A ASIC	
(Chips)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

Training Algorithm

SE Function

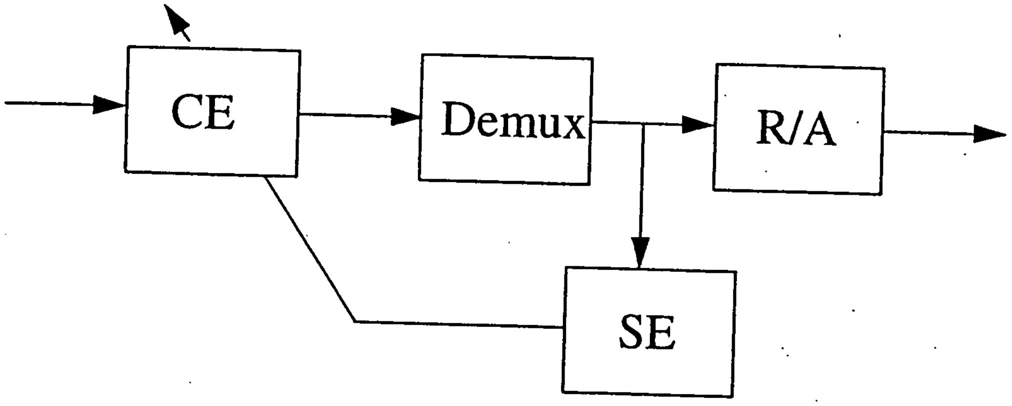
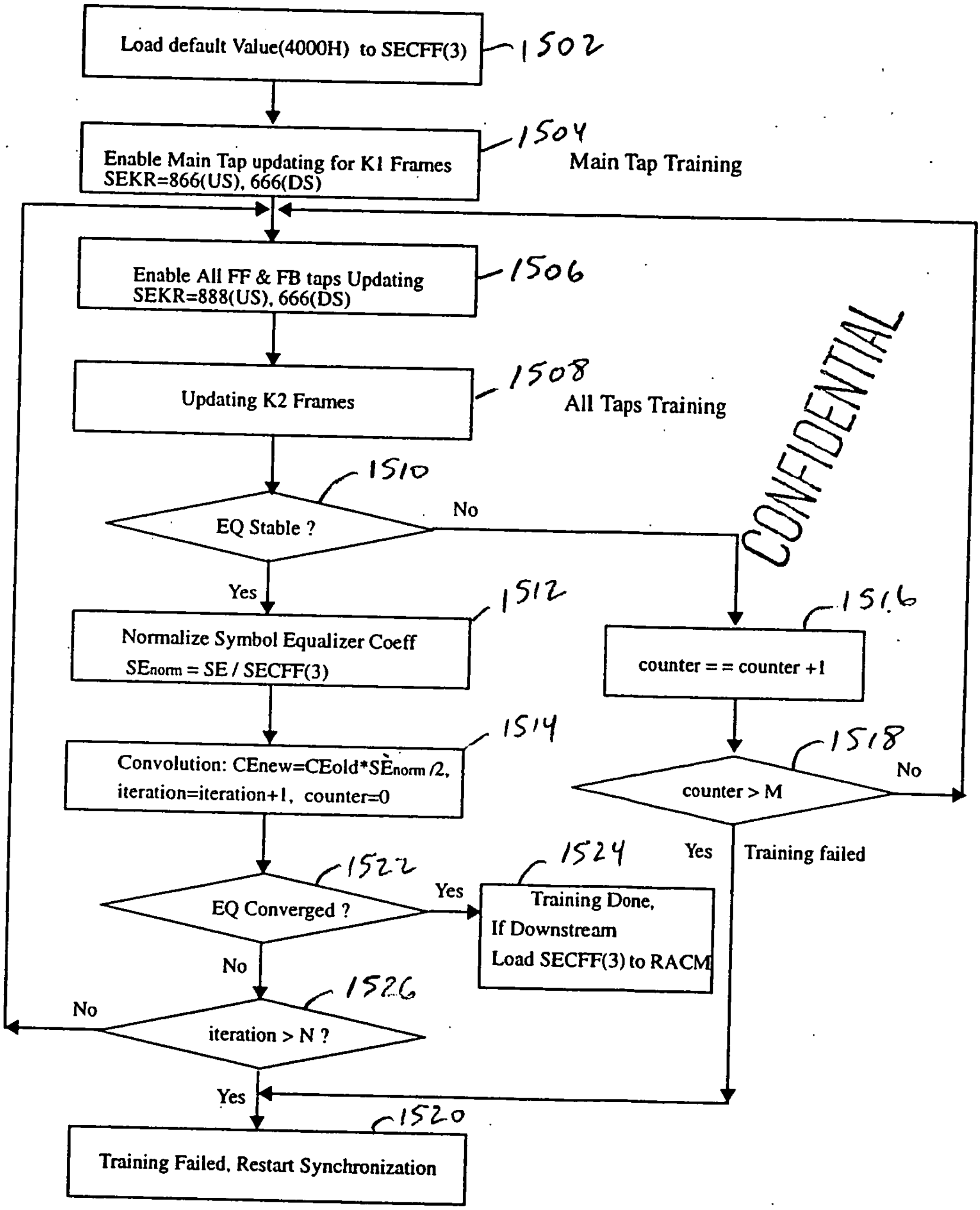


FIG. 59

Initial 2-Step Training Algorithm


Load default Value(4000H) to SECFF(3)
1502
Enable Main Tap updating for K1 Frames
SEKR=866(US), 666(DS)
1504
Main Tap Training
Enable All FF & FB taps Updating
SEKR=888(US), 666(DS)
1506
Updating K2 Frames
1508
All Taps Training
EQ Stable ?
1510
No
Yes
Normalize Symbol Equalizer Coeff
SE_{norm} = SE / SECFF(3)
1512
counter = = counter +1
1516
Convolution: CEnew=CEold*SE_{norm} /2,
iteration=iteration+1, counter=0
1514
counter > M
1518
No
Yes
Training failed
EQ Converged ?
1522
Yes
Training Done,
If Downstream
Load SECFF(3) to RACM
1524
No
iteration > N ?
1526
No
Yes
Training Failed, Restart Synchronization
1520

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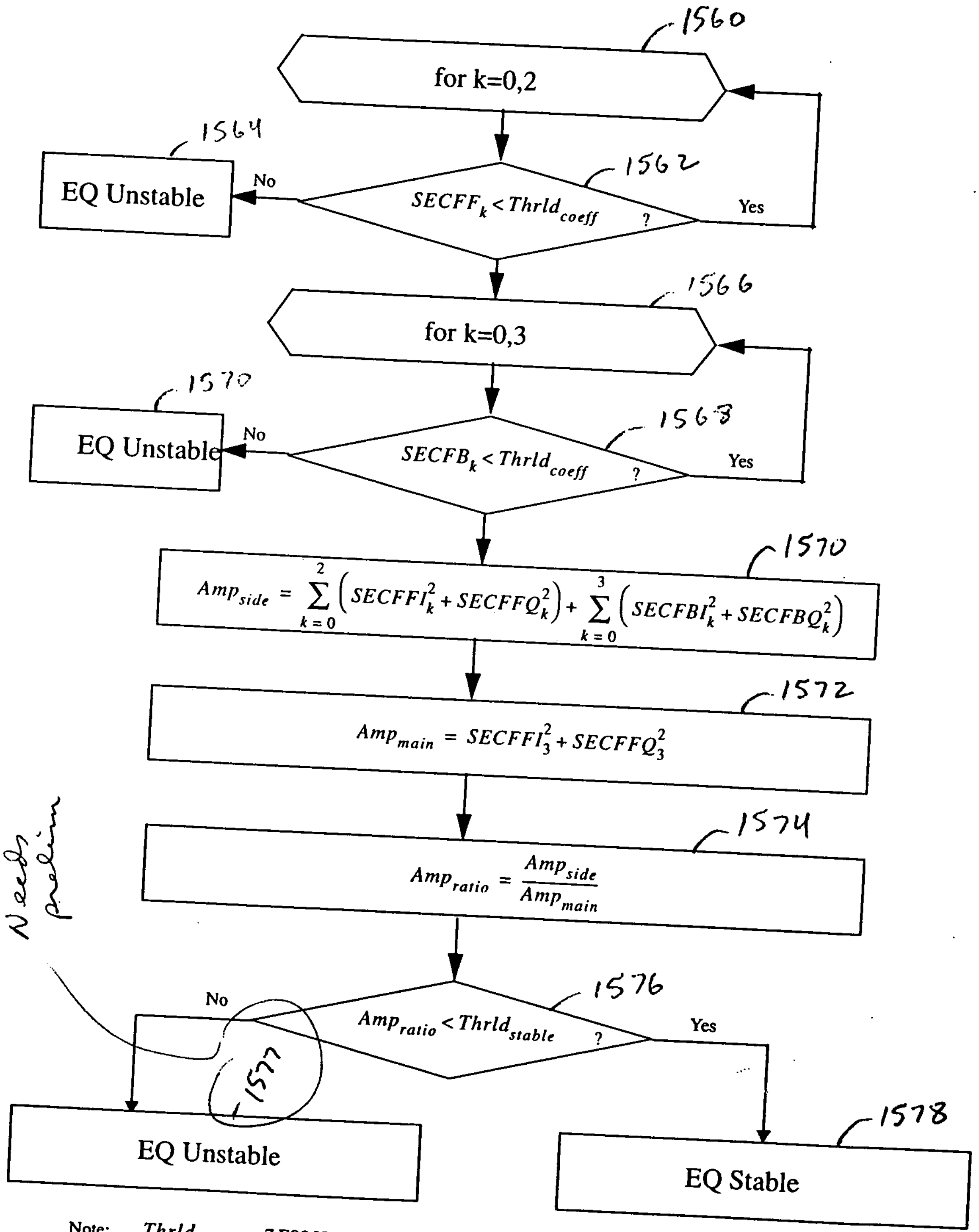
2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

EQ Stability Check


1560
for k=0,2
1564
EQ Unstable
No
$SECFF_k < Thrld_{coeff}$?
1562
Yes
1566
for k=0,3
1570
EQ Unstable
No
$SECFB_k < Thrld_{coeff}$?
1568
Yes
1570
$Amp_{side} = \sum_{k=0}^{2}\left(SECFFI_k^2 + SECFFQ_k^2\right) + \sum_{k=0}^{3}\left(SECFBI_k^2 + SECFBQ_k^2\right)$
1572
$Amp_{main} = SECFFI_3^2 + SECFFQ_3^2$
1574
$Amp_{ratio} = \frac{Amp_{side}}{Amp_{main}}$
Needs prelim
No
$Amp_{ratio} < Thrld_{stable}$?
1576
Yes
1577
EQ Unstable
1578
EQ Stable

Note: $Thrld_{coeff} = 7F00H$ $Thrld_{stable} = 10^{-3}$

FIG. 61

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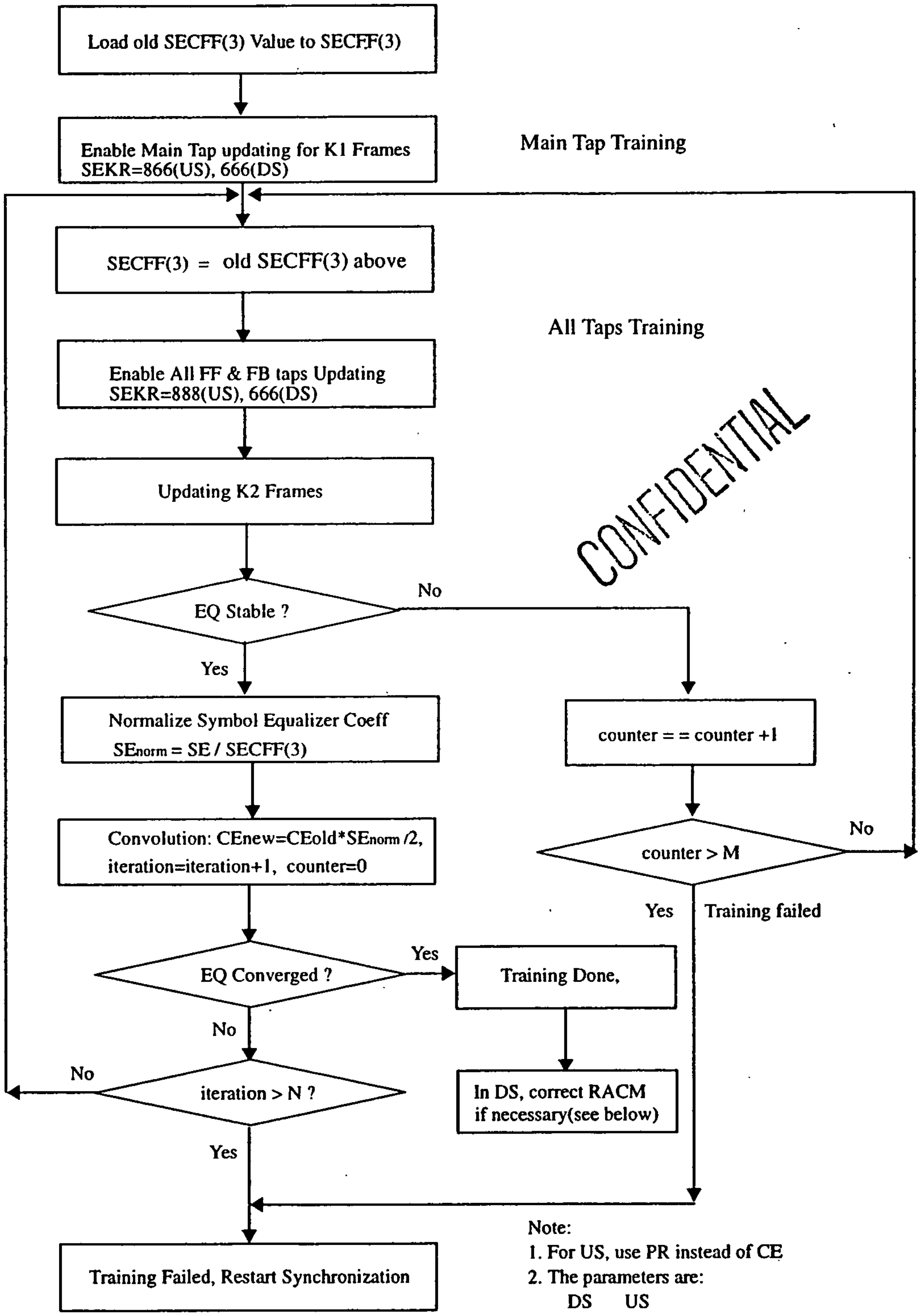
Periodic 2-Step Training Algorithm


Load old SECFF(3) Value to SECFF(3)
Enable Main Tap updating for K1 Frames
SEKR=866(US), 666(DS)
Main Tap Training
SECFF(3) = old SECFF(3) above
All Taps Training
Enable All FF & FB taps Updating
SEKR=888(US), 666(DS)
Updating K2 Frames
EQ Stable ?
No
Yes
Normalize Symbol Equalizer Coeff
SEnorm = SE / SECFF(3)
counter = = counter +1
Convolution: CEnew=CEold*SEnorm /2,
iteration=iteration+1, counter=0
counter > M
No
Yes
Training failed
EQ Converged ?
Yes
Training Done,
No
No
iteration > N ?
In DS, correct RACM
if necessary(see below)
Yes
Training Failed, Restart Synchronization

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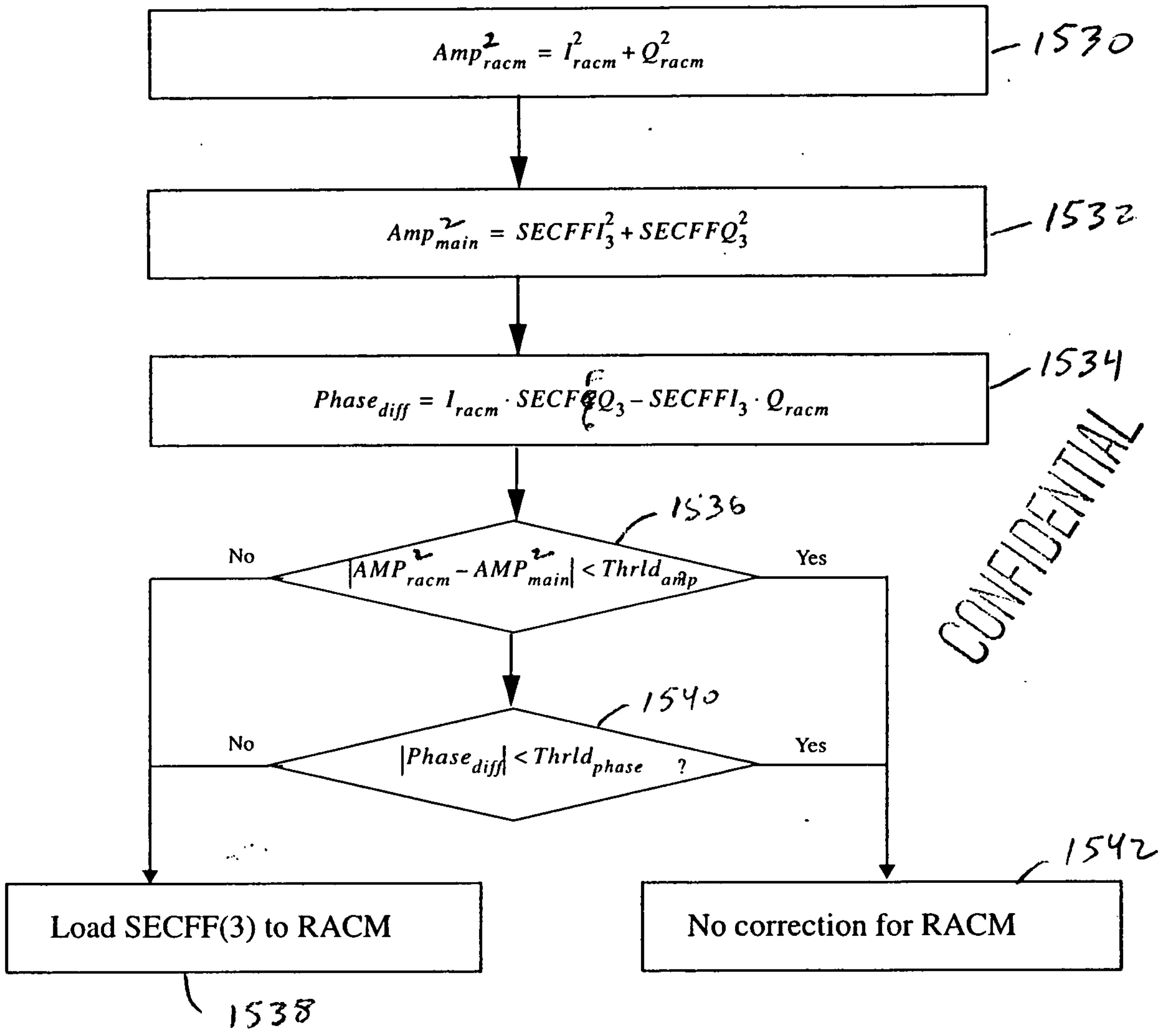
Note:
1. For US, use PR instead of CE
2. The parameters are:

	DS	US
K1	30	30
K2	20	30
N	5	3
M	3	3

FIG. 62

RACM Correction



$Amp^2_{racm} = I^2_{racm} + Q^2_{racm}$
1530
$Amp^2_{main} = SECFFI^2_3 + SECFFQ^2_3$
1532
$Phase_{diff} = I_{racm} \cdot SECFFQ_3 - SECFFI_3 \cdot Q_{racm}$
1534
1536
No
$|AMP^2_{racm} - AMP^2_{main}| < Thrld_{amp}$
Yes
1540
No
$|Phase_{diff}| < Thrld_{phase}$?
Yes
1542
Load SECFF(3) to RACM
No correction for RACM
1538

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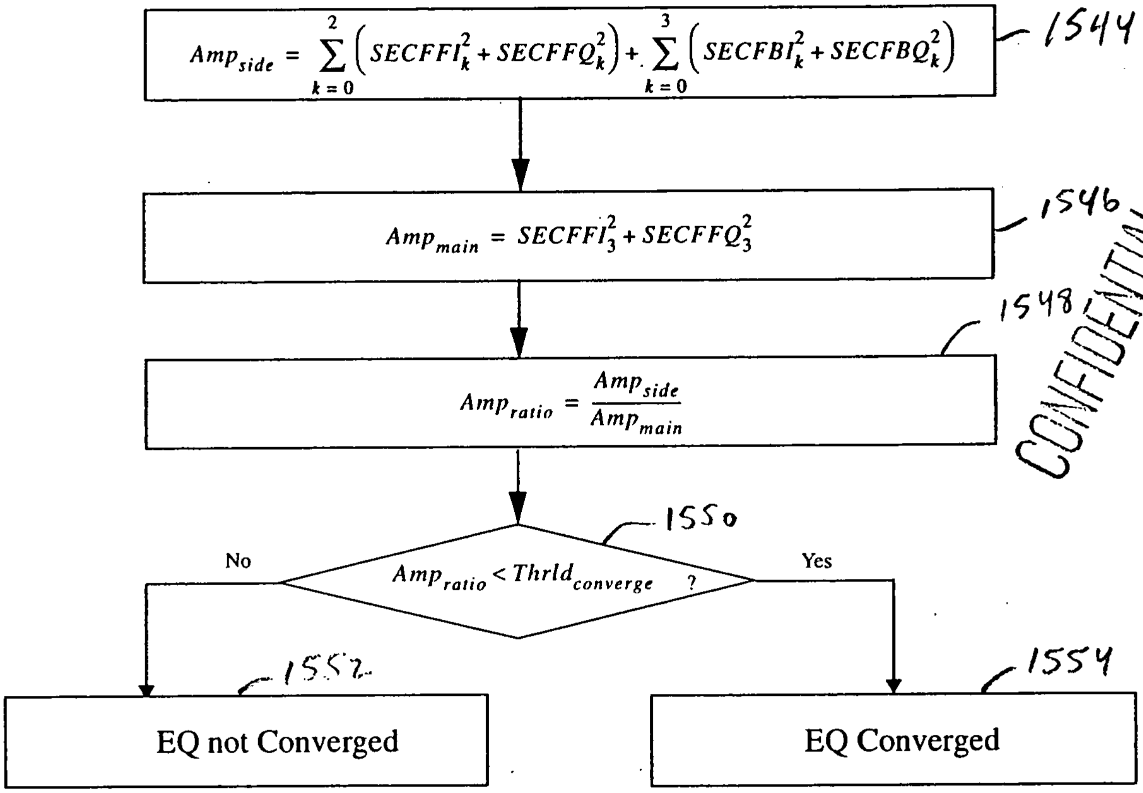
Note: $Thrld_{amp} = TBD$

$Thrld_{phase} = TBD$

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

EQ Convergence Check


$Amp_{side} = \sum_{k=0}^{2}\left(SECFFI_k^2 + SECFFQ_k^2\right) + \sum_{k=0}^{3}\left(SECFBI_k^2 + SECFBQ_k^2\right)$
1544
$Amp_{main} = SECFFI_3^2 + SECFFQ_3^2$
1546
1548
$Amp_{ratio} = \frac{Amp_{side}}{Amp_{main}}$
1550
$Amp_{ratio} < Thrld_{converge}$?
No
Yes
1552
1554
EQ not Converged
EQ Converged

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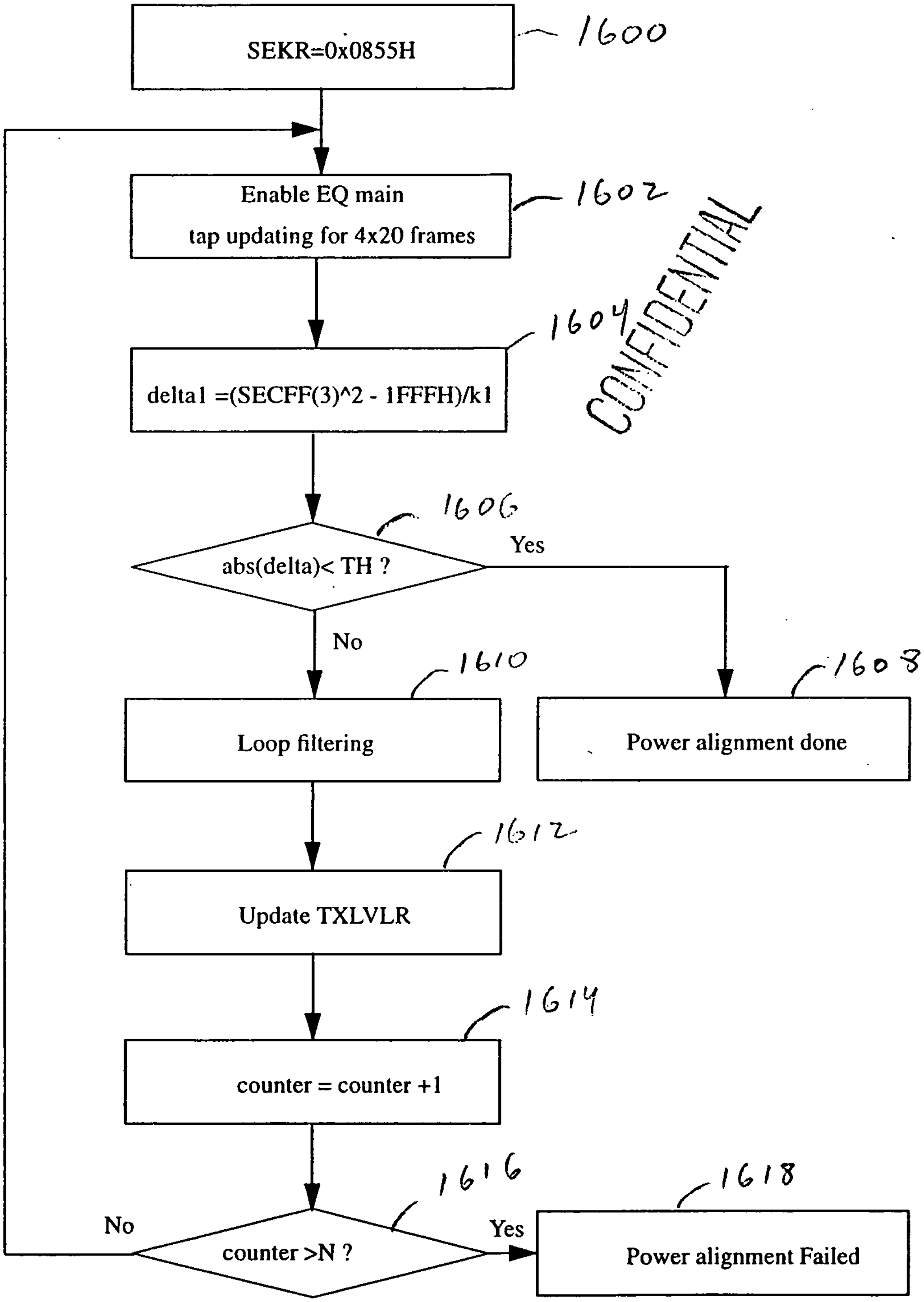
Note: $Thrld_{converge} = 10^{-5}$

FIG. 64

Power Alignment Flow Chart


SEKR=0x0855H
1600
Enable EQ main tap updating for 4x20 frames
1602
delta1 =(SECFF(3)^2 - 1FFFH)/k1
1604
abs(delta)< TH ?
1606
Yes
No
Loop filtering
1610
Power alignment done
1608
Update TXLVLR
1612
counter = counter +1
1614
counter >N ?
1616
No
Yes
Power alignment Failed
1618

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Note: TH = 600H
N = 12

FIG. 65

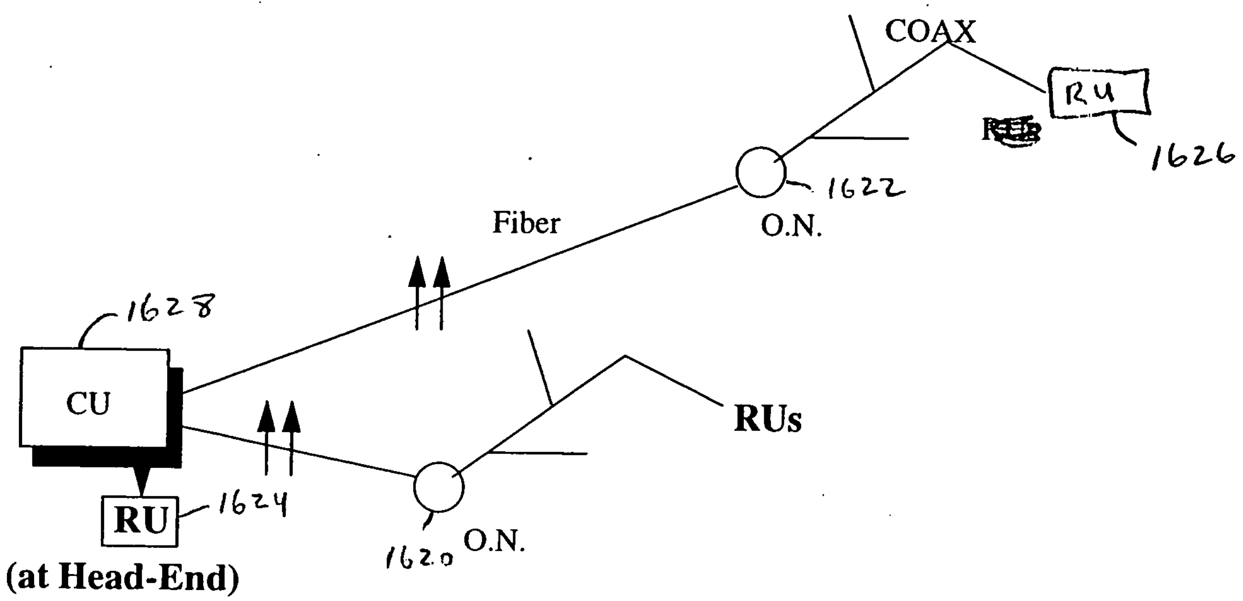
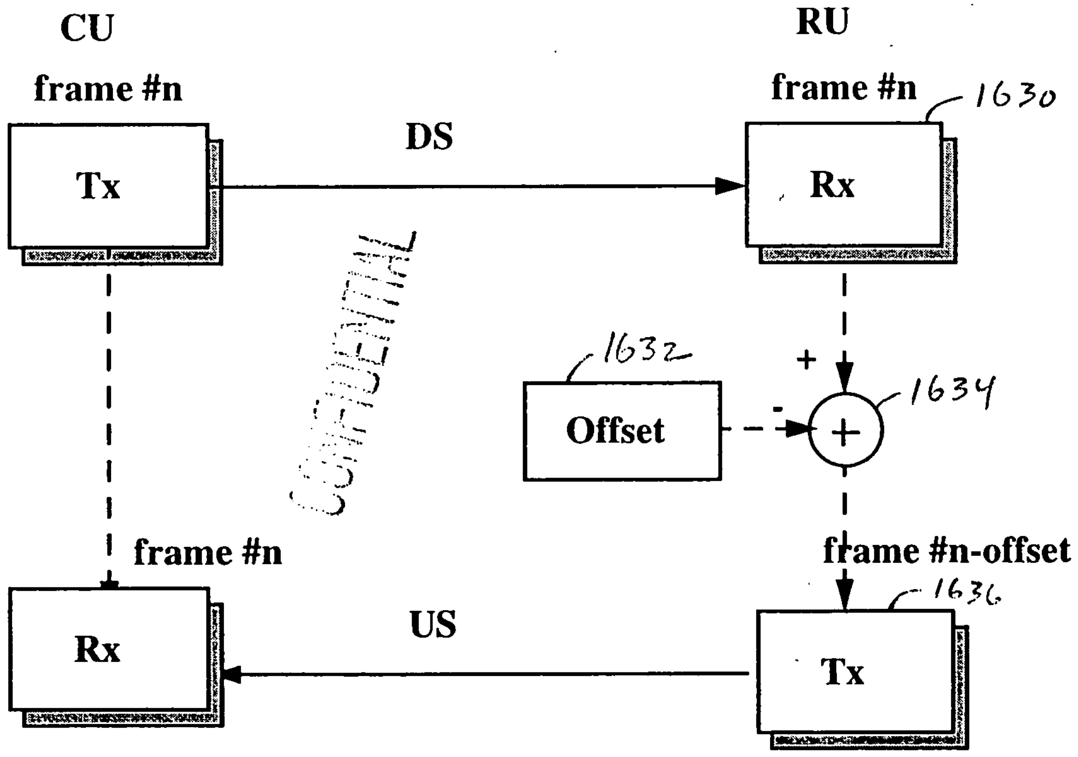

COAX
RU
1626
Fiber
1622
O.N.
1628
CU
RUs
RU
1624
(at Head-End)
1620
O.N.

FIG. 66


CU
frame #n
Tx
DS
RU
frame #n
1630
Rx
1632
Offset
+
-
+
1634
frame #n
frame #n-offset
1636
Rx
US
Tx

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Total Turn Around (TTA) in frames = Offset

FIG. 67

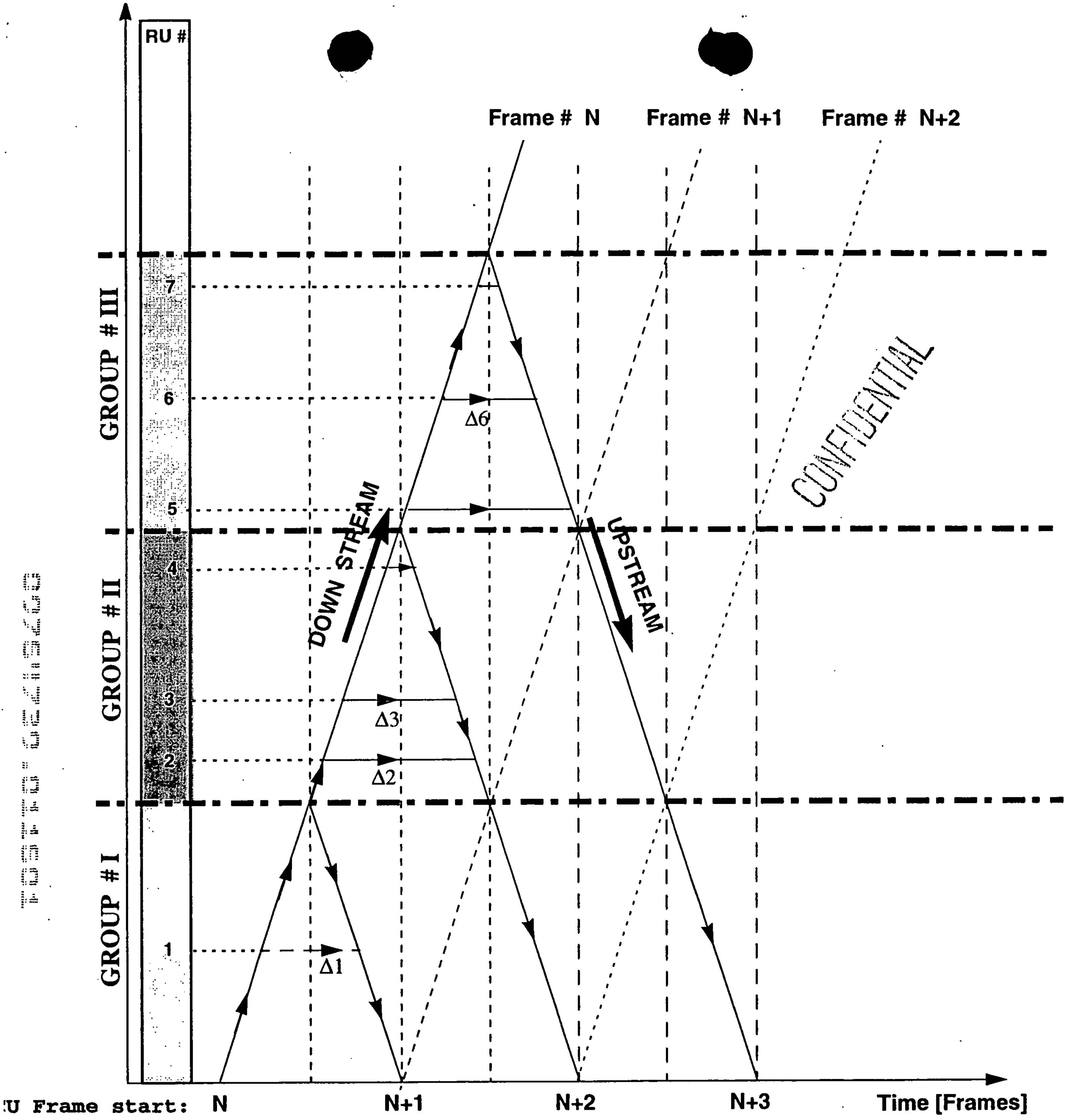
RU #
Frame # N
Frame # N+1
Frame # N+2
GROUP # III
GROUP # II
GROUP # I
7
6
5
4
3
2
1
Δ6
Δ3
Δ2
Δ1
DOWN STREAM
UPSTREAM
U Frame start:
N
N+1
N+2
N+3
Time [Frames]

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FIG. 68

~~Figure 3.1: Frame start propagation along the channel~~

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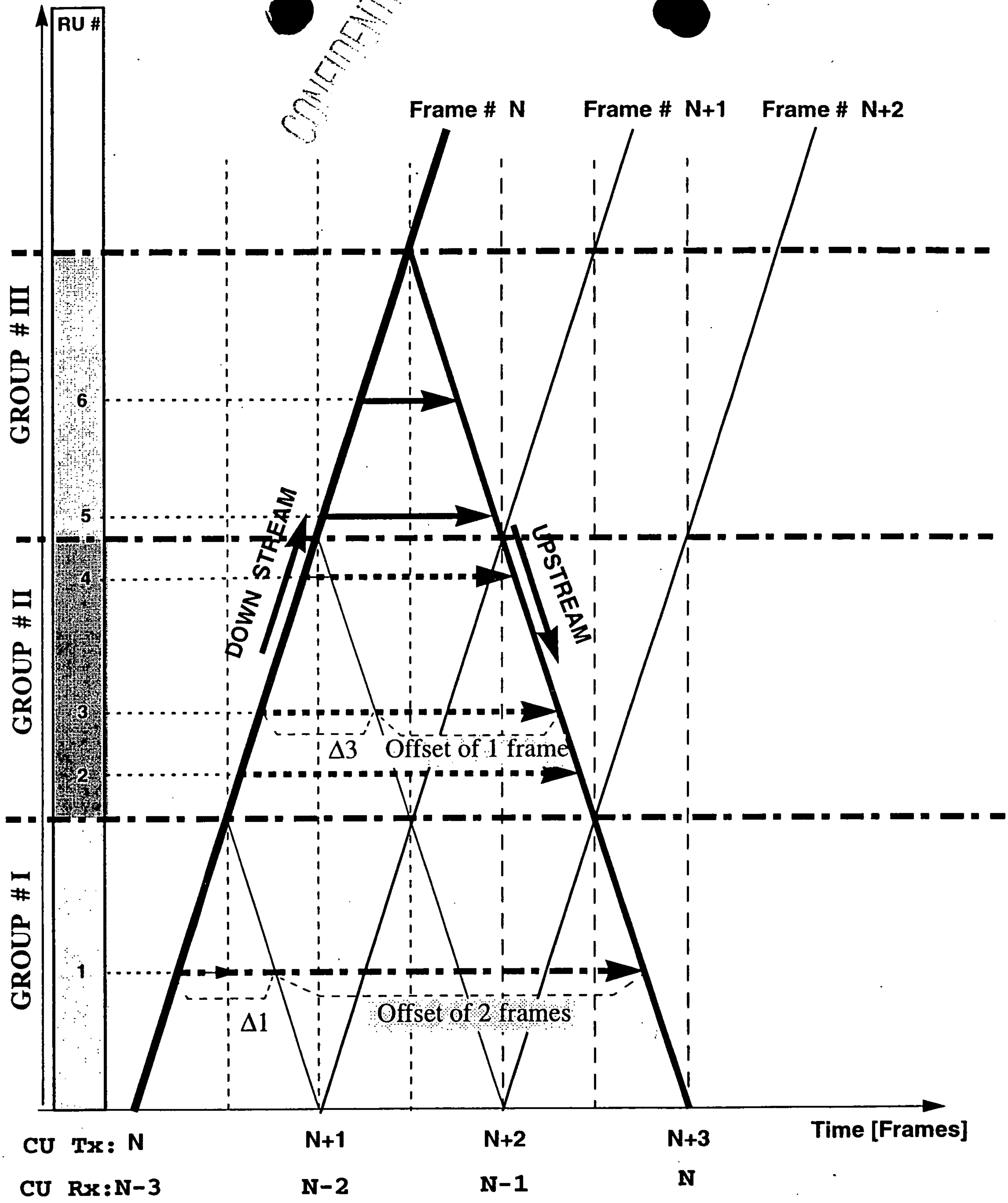

RU #
Frame # N
Frame # N+1
Frame # N+2
GROUP # III
GROUP # II
GROUP # I
6
5
4
3
2
1
DOWN STREAM
UPSTREAM
Δ3
Offset of 1 frame
Δ1
Offset of 2 frames
CU Tx: N
N+1
N+2
N+3
Time [Frames]
CU Rx: N-3
N-2
N-1
N

FIG. 69

[redacted] Control message (downstream) and function (upstream) propagation in a 3 frames TTA channel

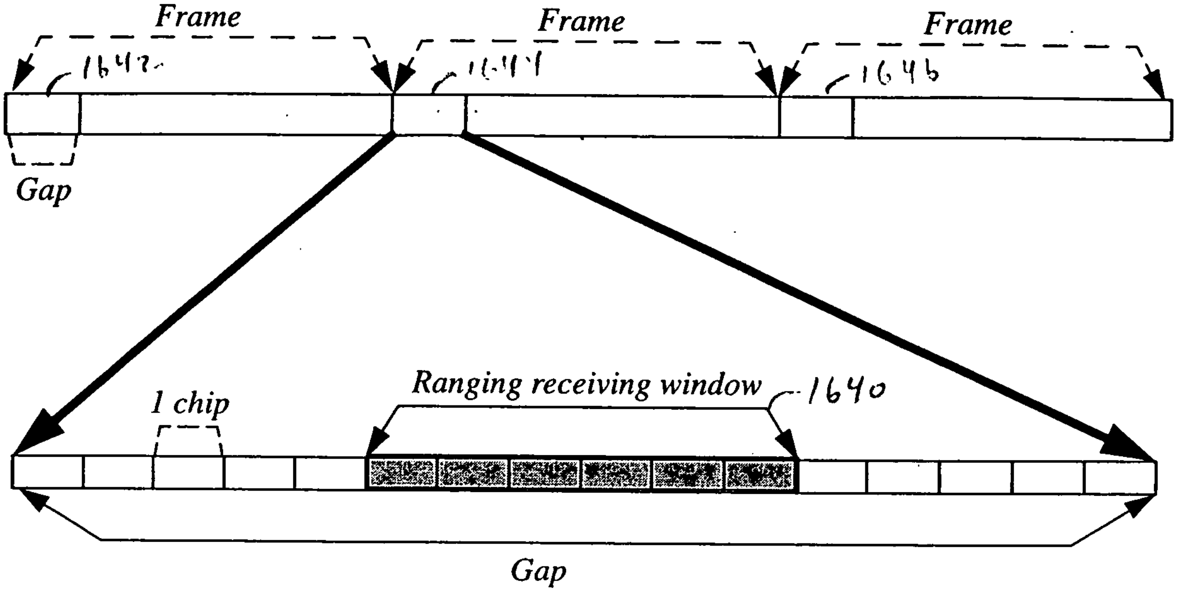
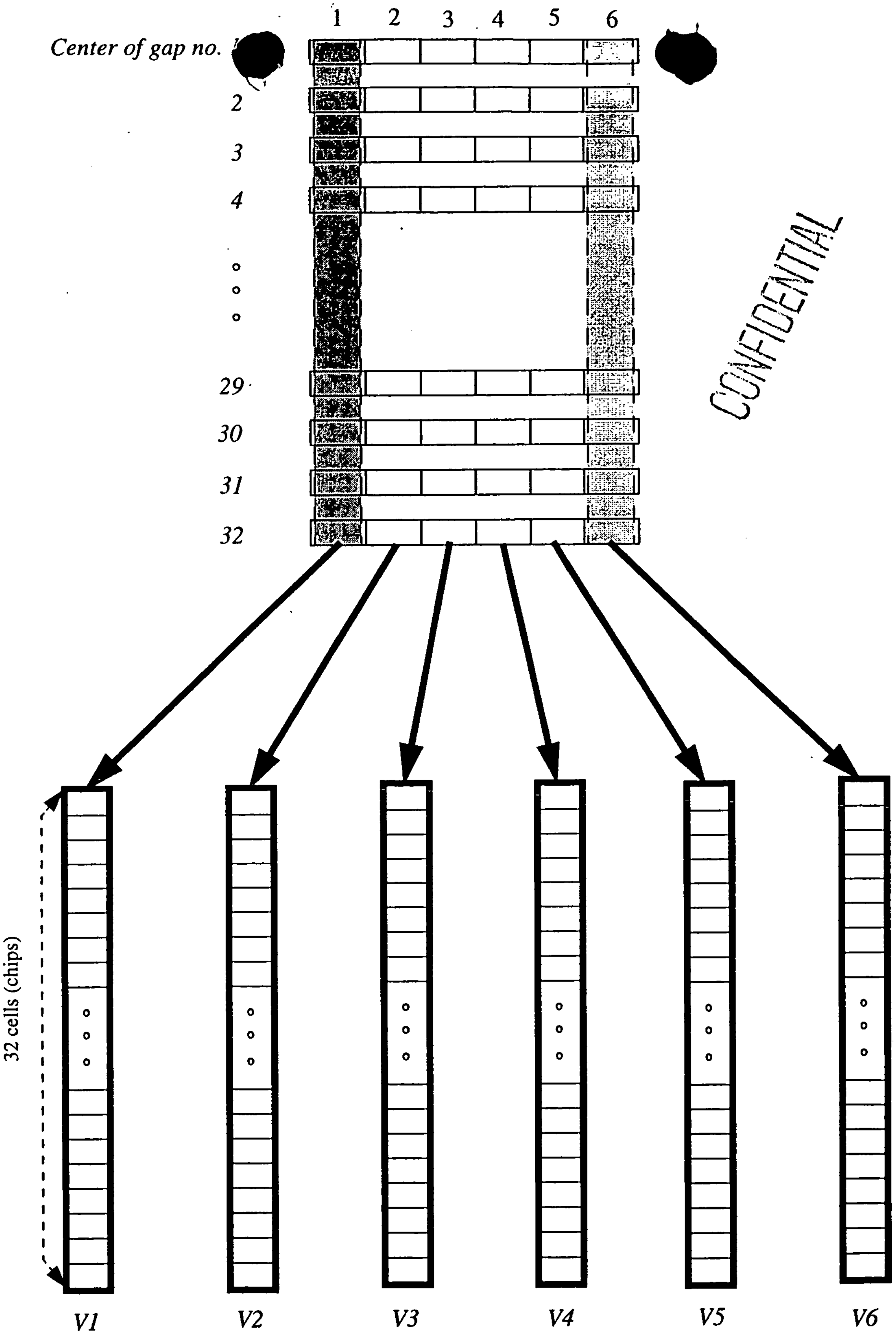

Frame
Frame
Frame
1642
1644
1646
Gap
1 chip
Ranging receiving window
1640
Gap

FIG. 70


1
2
3
4
5
6
Center of gap no. 1
2
3
4
29
30
31
32
32 cells (chips)
V1
V2
V3
V4
V5
V6

CONFIDENTIAL

Figure 3.4: Overall view of the CU sensing windows in a "boundless ranging" algorithm

FIG. 71

6

Chip\FR	**1**	**2**	**3**	**4**	**5**	**6**	**7**		**33**
1	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**...**	**0**
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72

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